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MS-7510

Version : 1.0 **acer** Beetle

CPU :

Intel Wolfield Family and Yorkfield Family Processor
Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 and 500 Sequence

System Chipset :

nVidia C72XE [C55 + BR04]
nVidia MCP55P



On Board Chipset :

Azalia Codec -- RealTek ALC888S
GB LAN 1 -- MARVELL/88E8056
GB LAN 2 -- MARVELL/88E8056
VRM 11 -- Intersil ISL6322
ACPI Controller -- uPI Solution
IEEE 1394a Controller -- JMicron JMB381
eSATA Controller -- JMicron JMB363
Super I/O -- ITE/IT8718F
SPI Flash 8Mb



Main Memory :

2 Channel DDR II * 4 (Max 8GB)

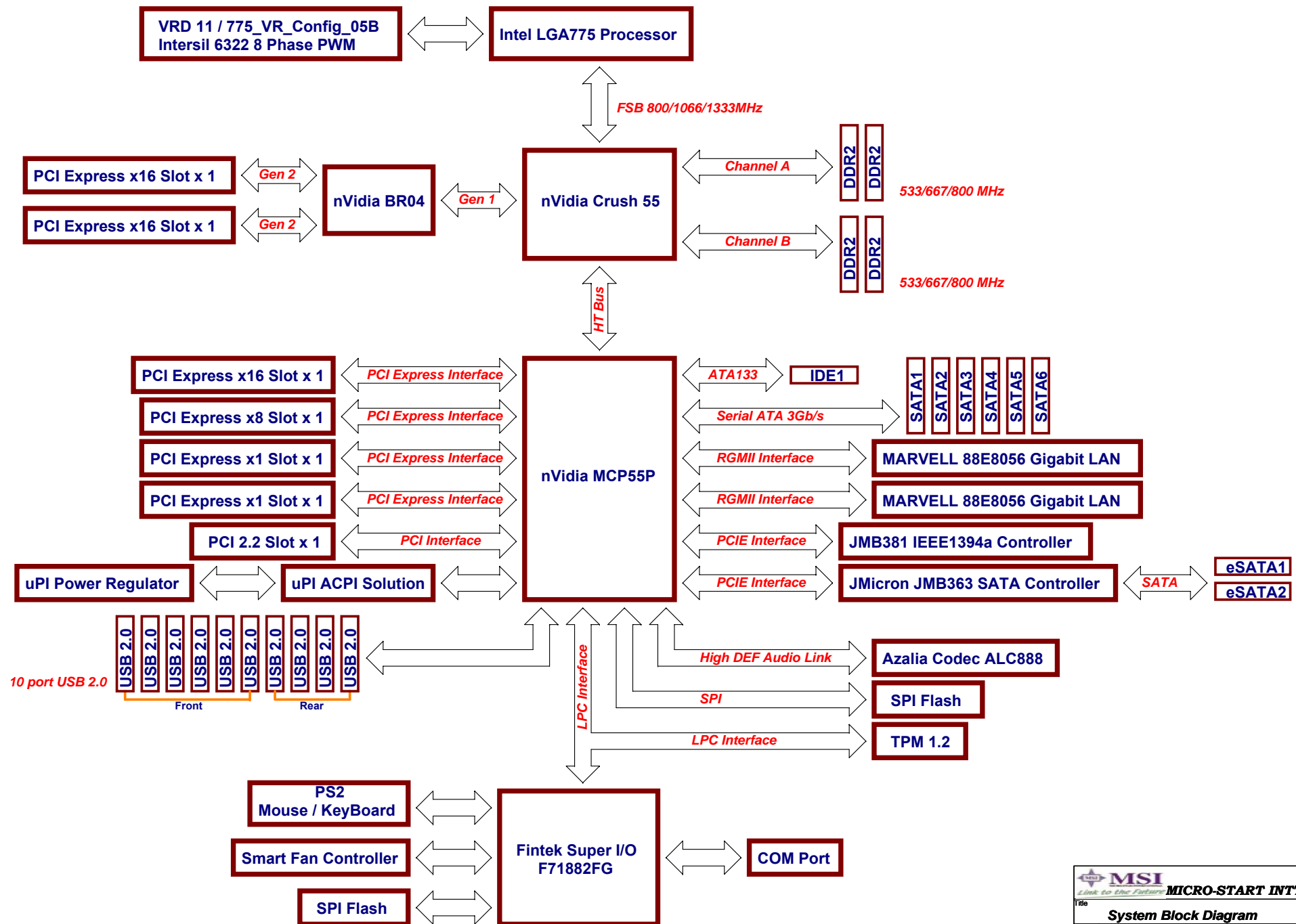
Expansion Slot :

PCI Express x16 Slot * 3
PCI Express x8 Slot * 1
PCI Express x1 Slot * 2
PCI Slot * 1

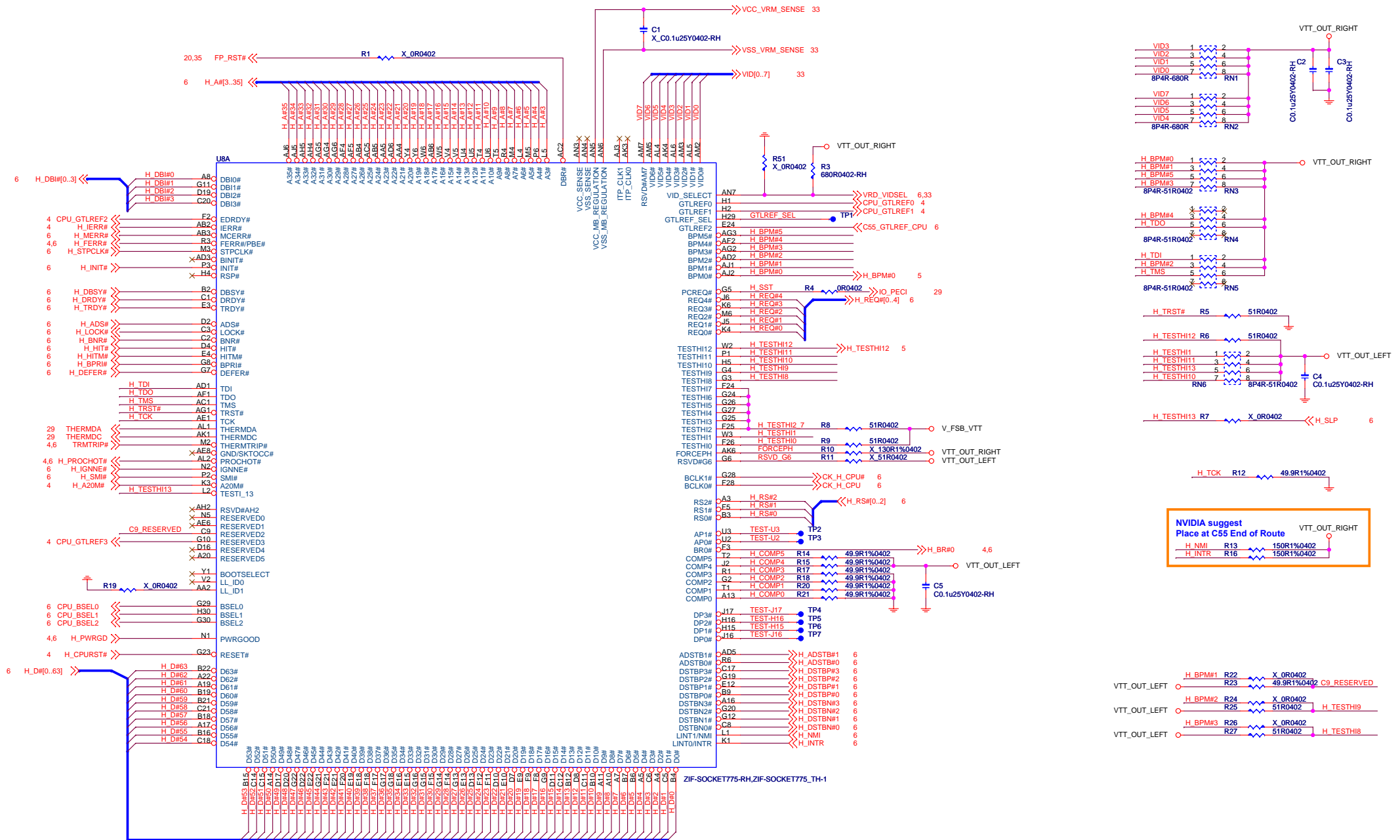


ERP No.	Config Item	PlatForm or Option	Option Select
	Cfg-STD	C55 + BR04 + MCP55P + ALC888S + MARVELL/88E8056 + JMB381 + JMB363 + ITE/IT8718F	STD

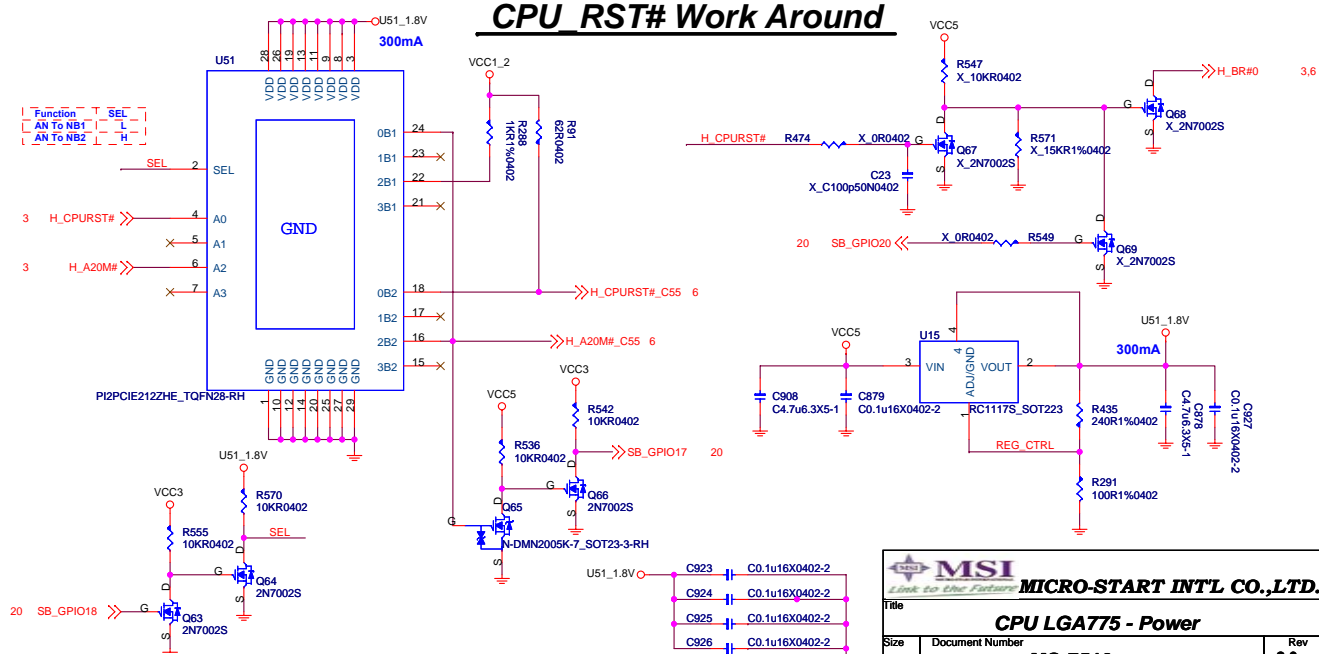
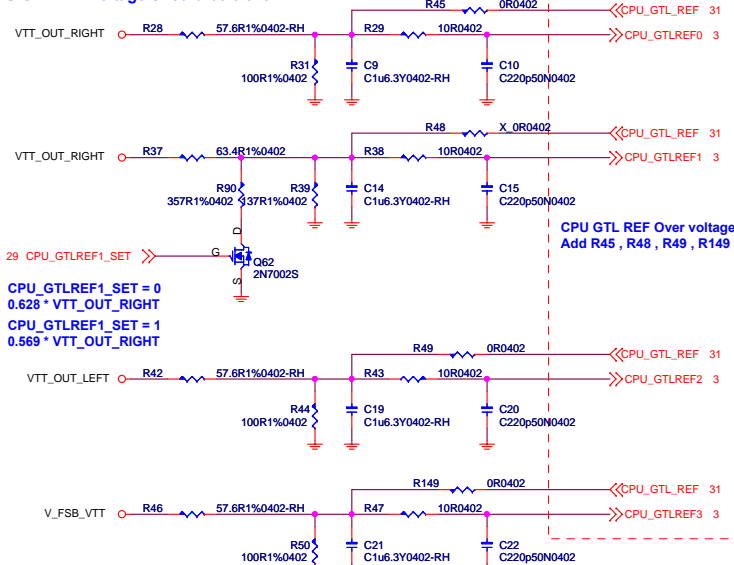
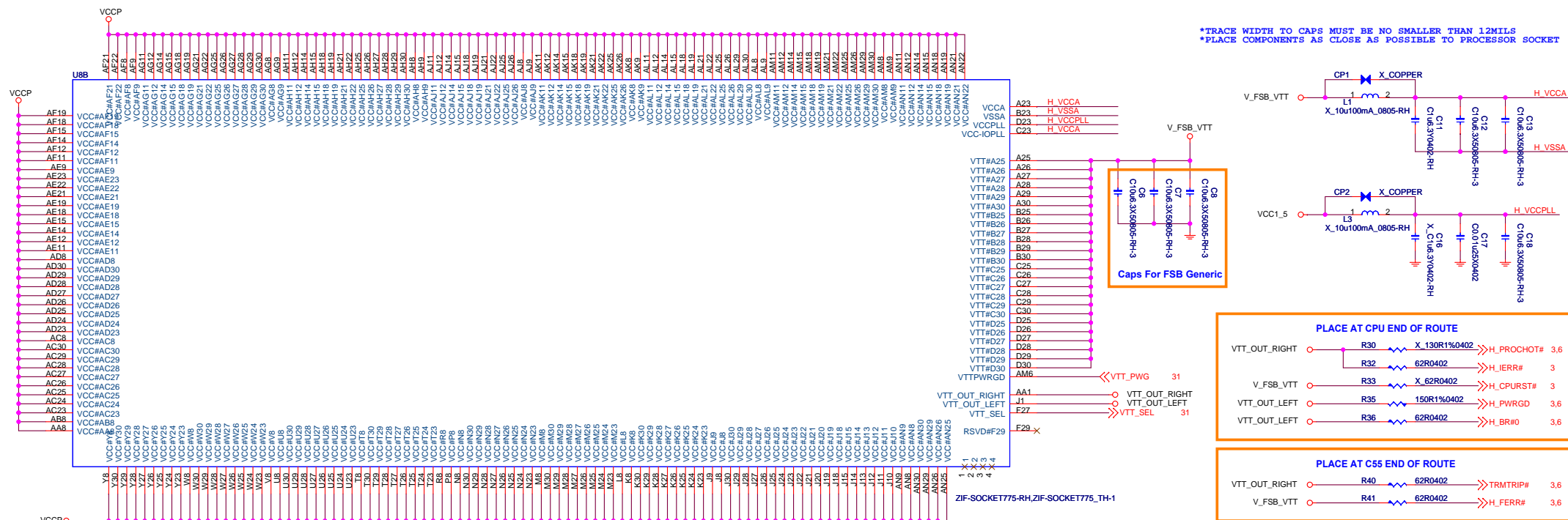
System Block Diagram



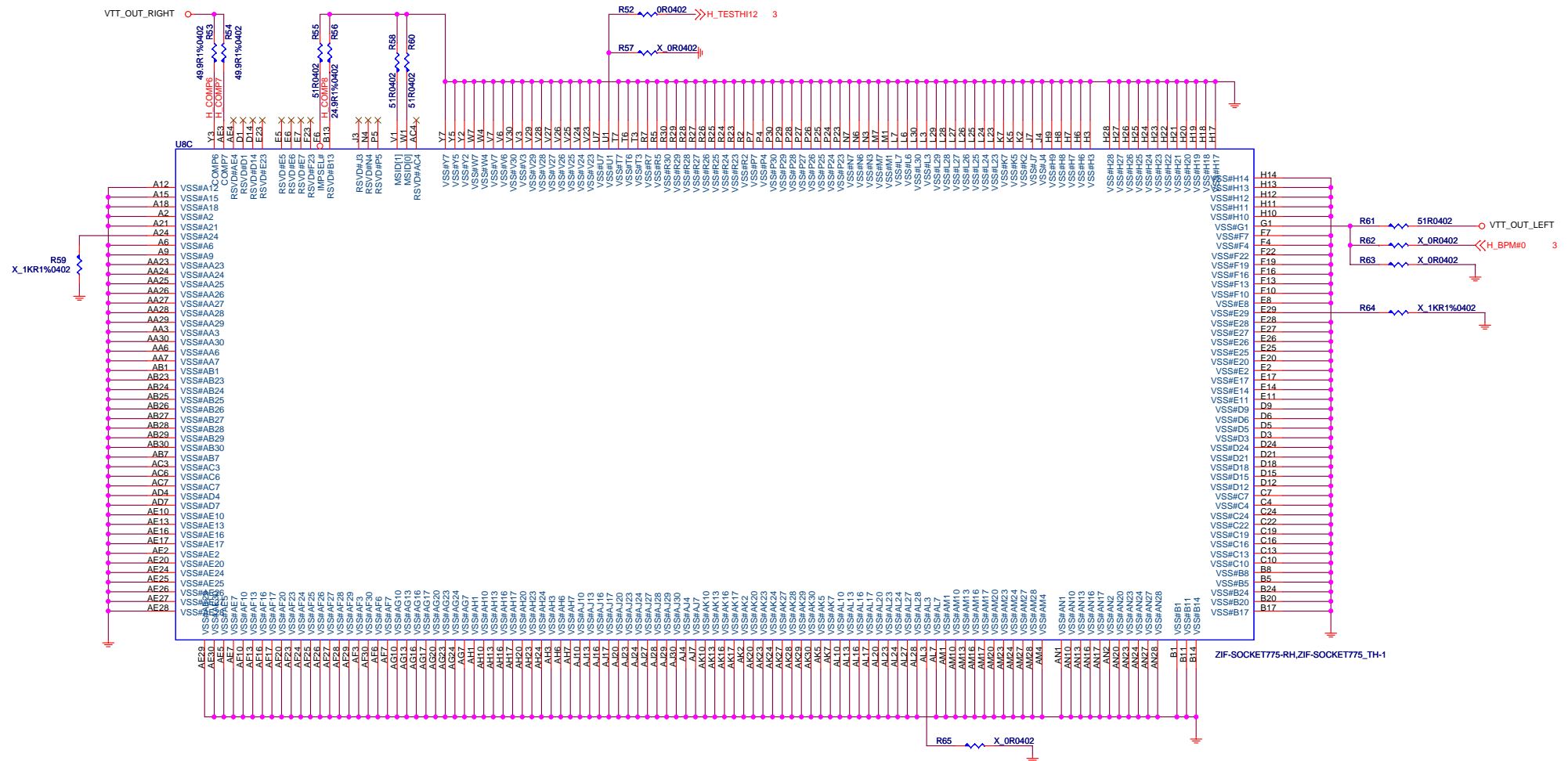
CPU LGA775 - Signals



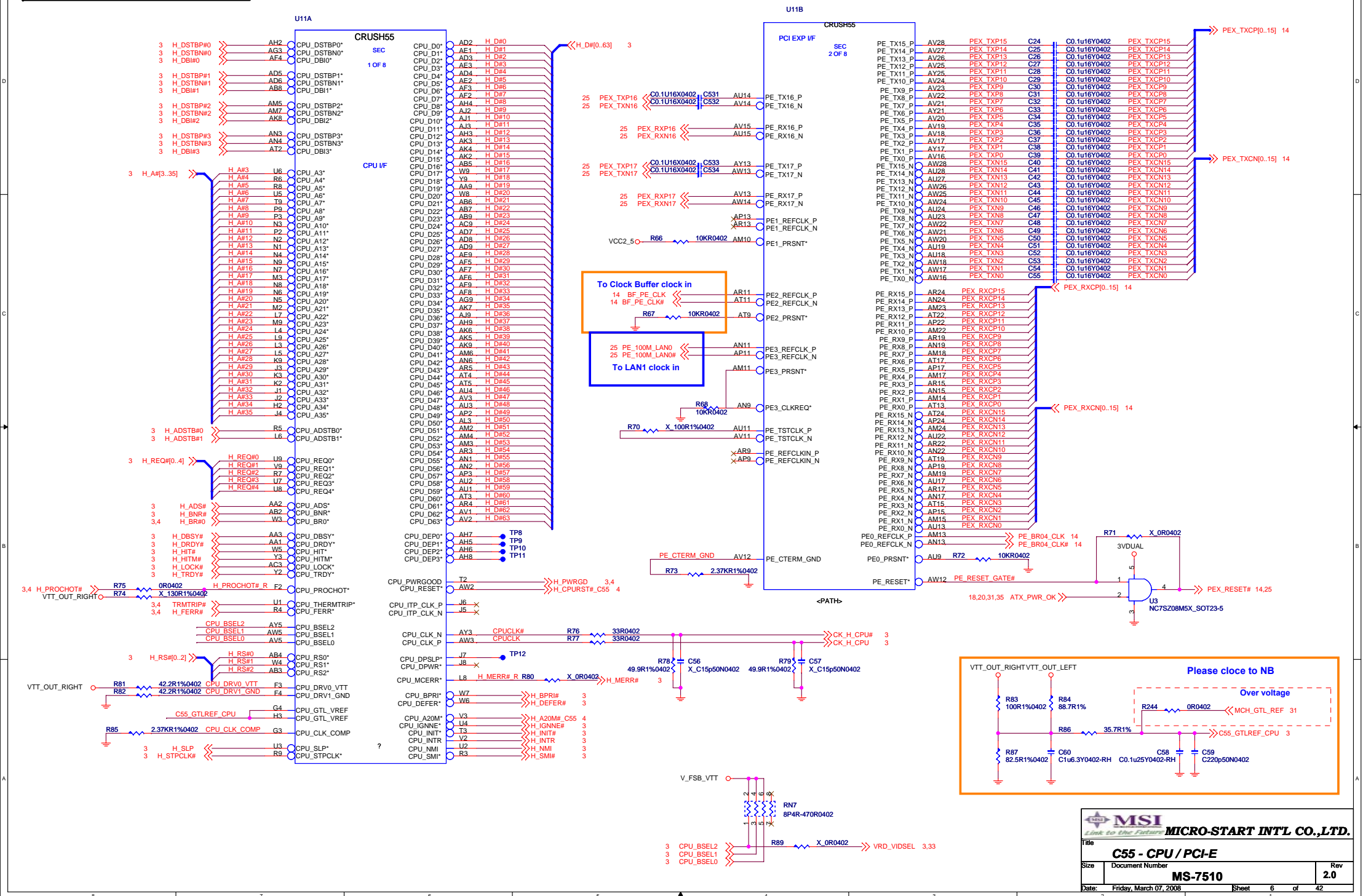
CPU LGA775 - Power



CPU LGA775 - Gnd

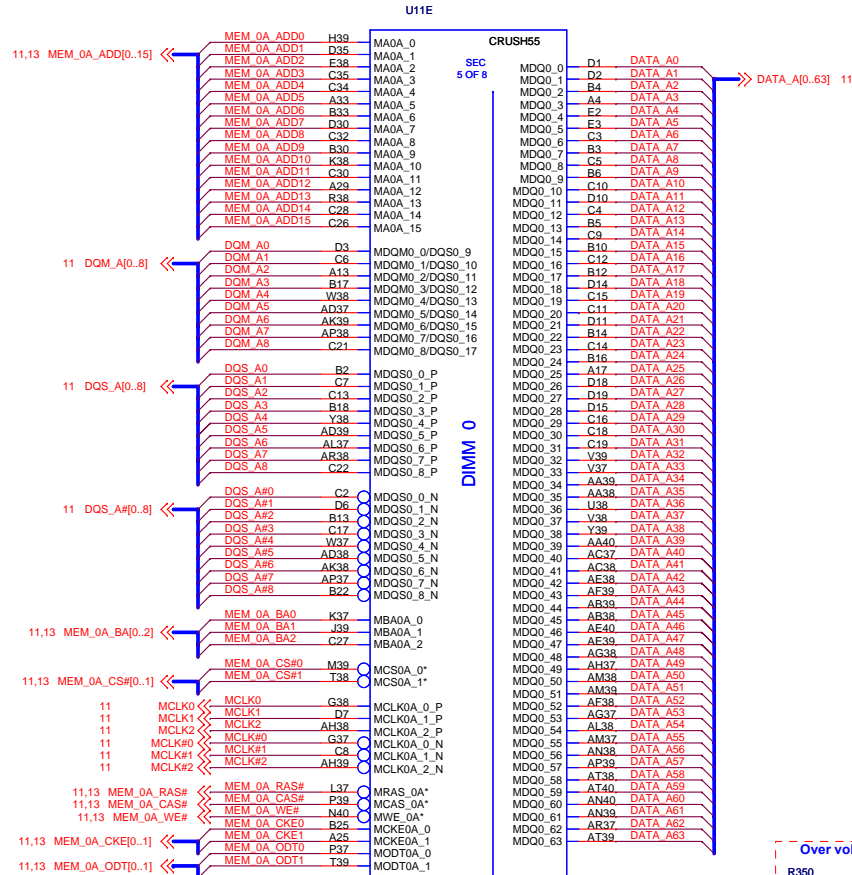


C55 - CPU / PCI-E

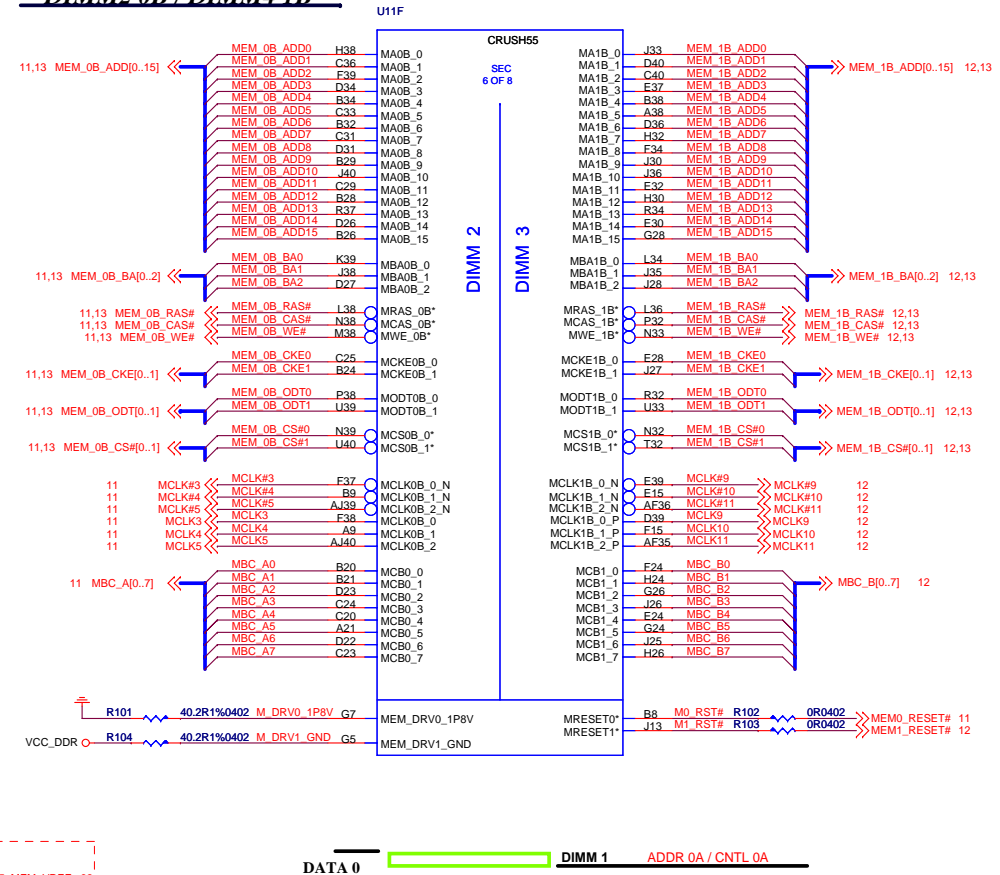


C55 - Memory A0

DIMM1 0A



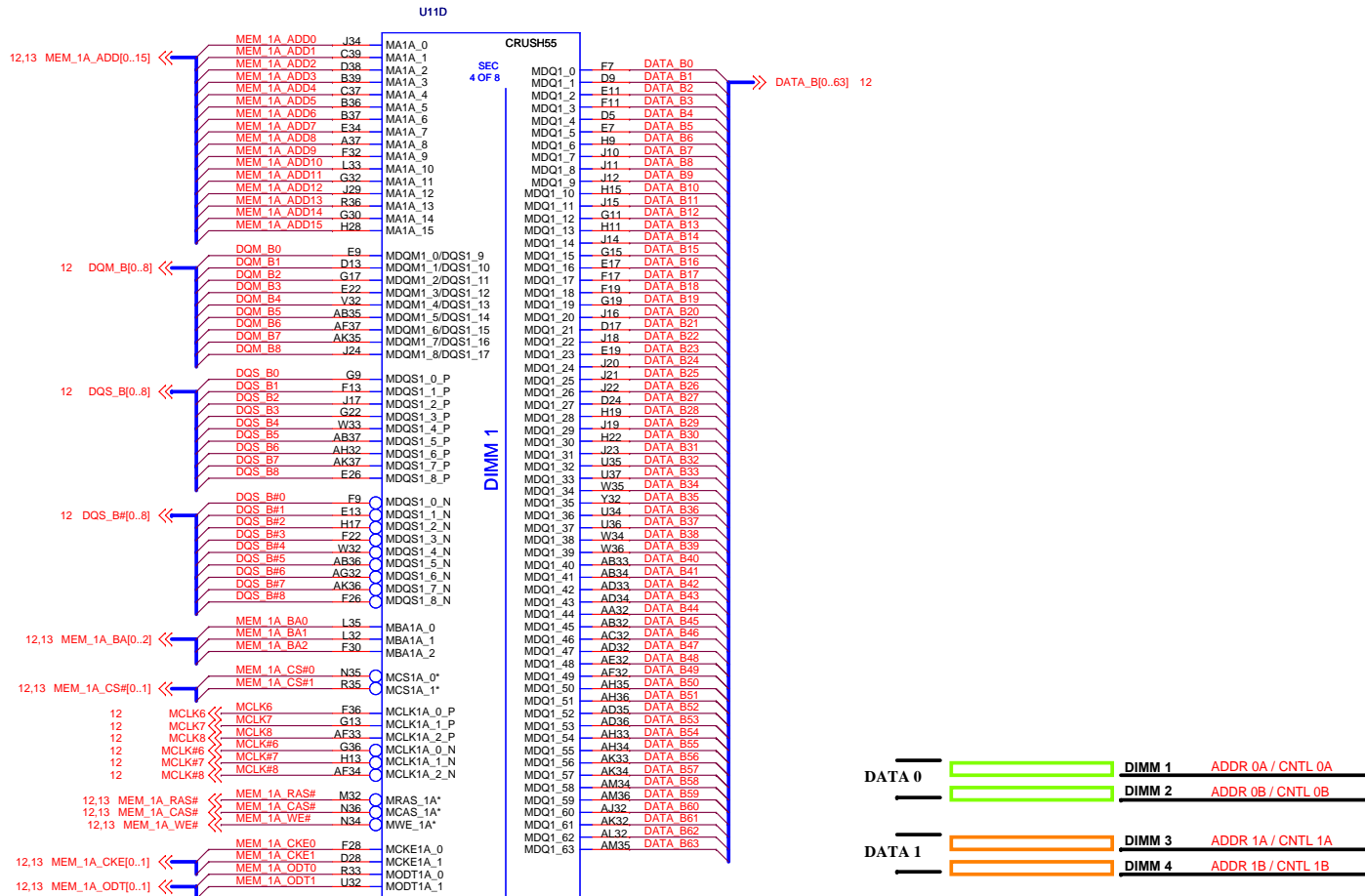
DIMM2 0B / DIMM4 1B



DATA 0	DIMM 1	ADDR 0A / CNTL 0A
	DIMM 2	ADDR 0B / CNTL 0B
DATA 1	DIMM 3	ADDR 1A / CNTL 1A
	DIMM 4	ADDR 1B / CNTL 1B

C55 - Memory A1

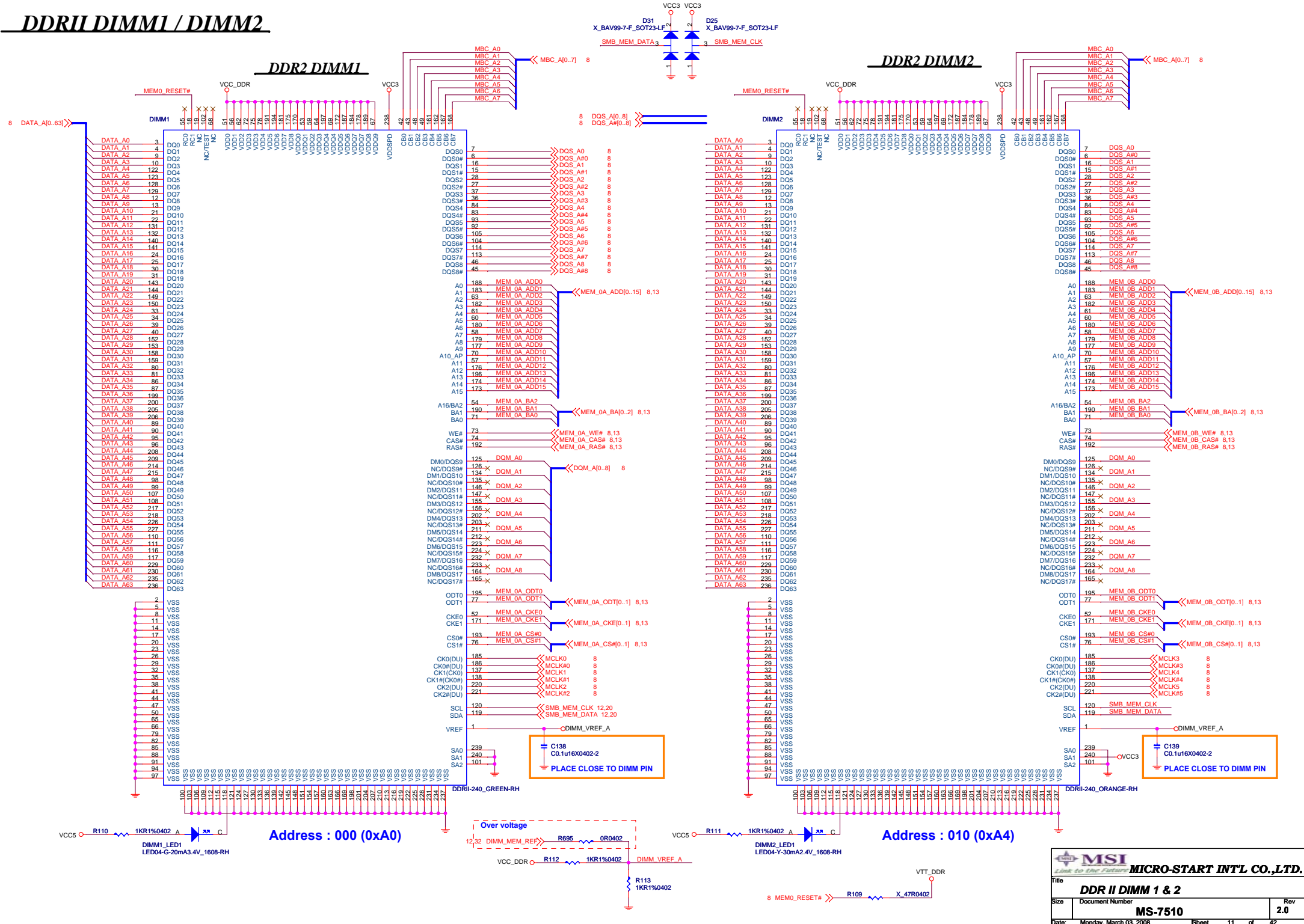
DIMM3 1A



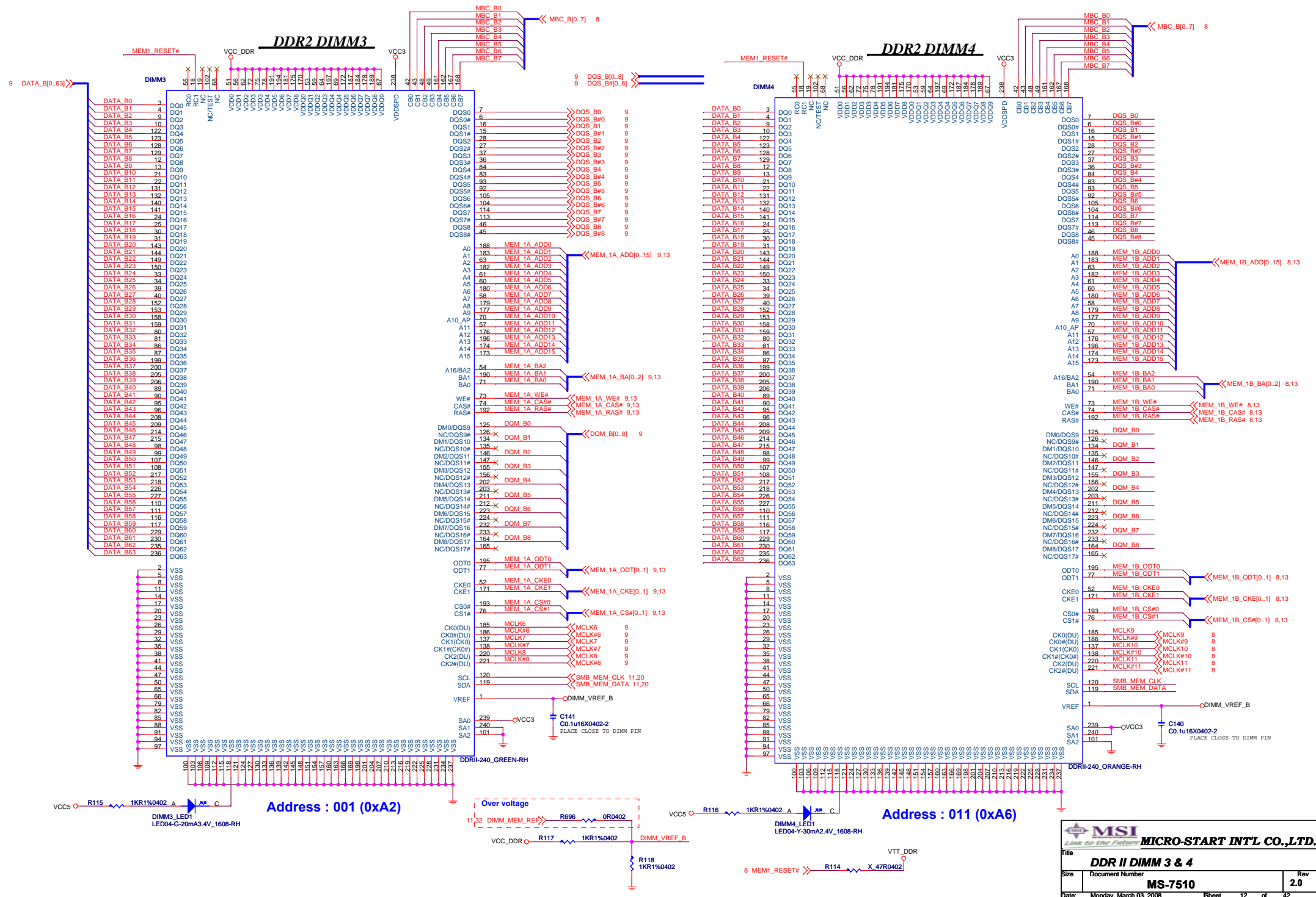
C55 - Gnd



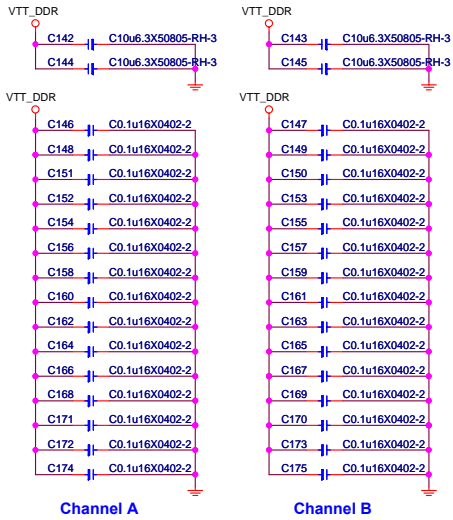
DDR1 DIMM1 / DIMM2



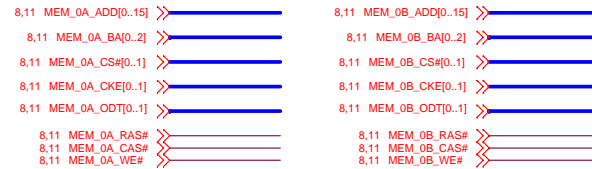
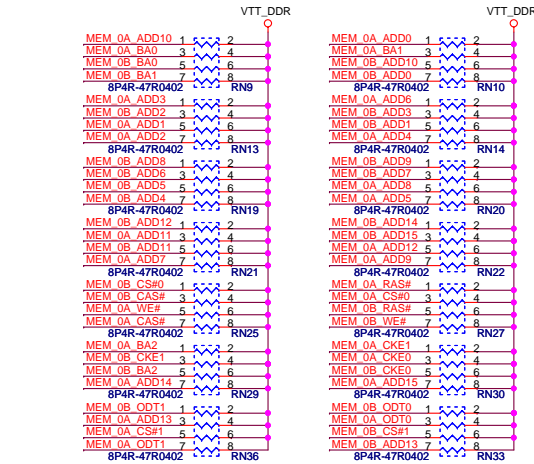
DDR II DIMM3 / DIMM4



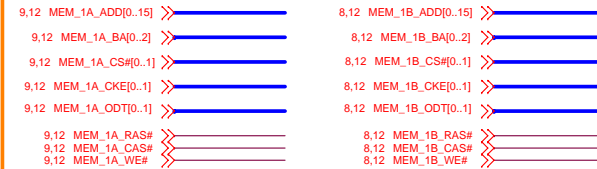
DDR Channel A VTT_DDR Decoupling Caps.



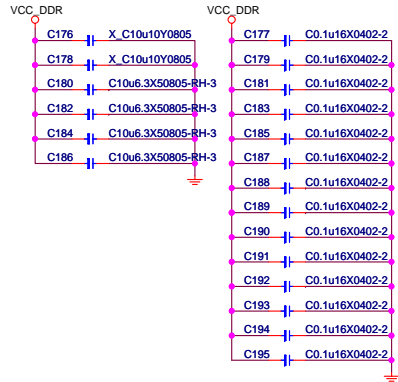
DDR Channel A Termination



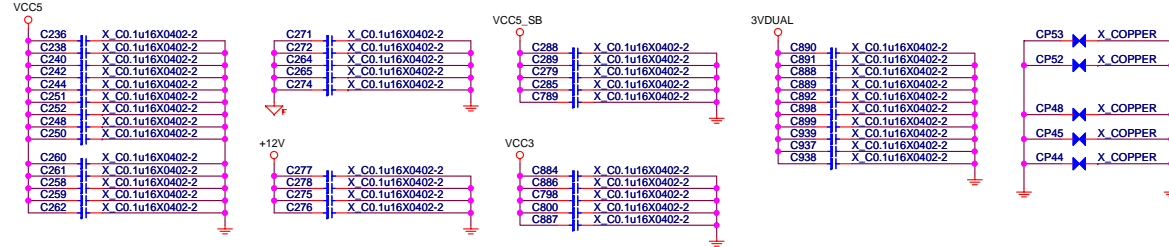
DDR Channel B Termination



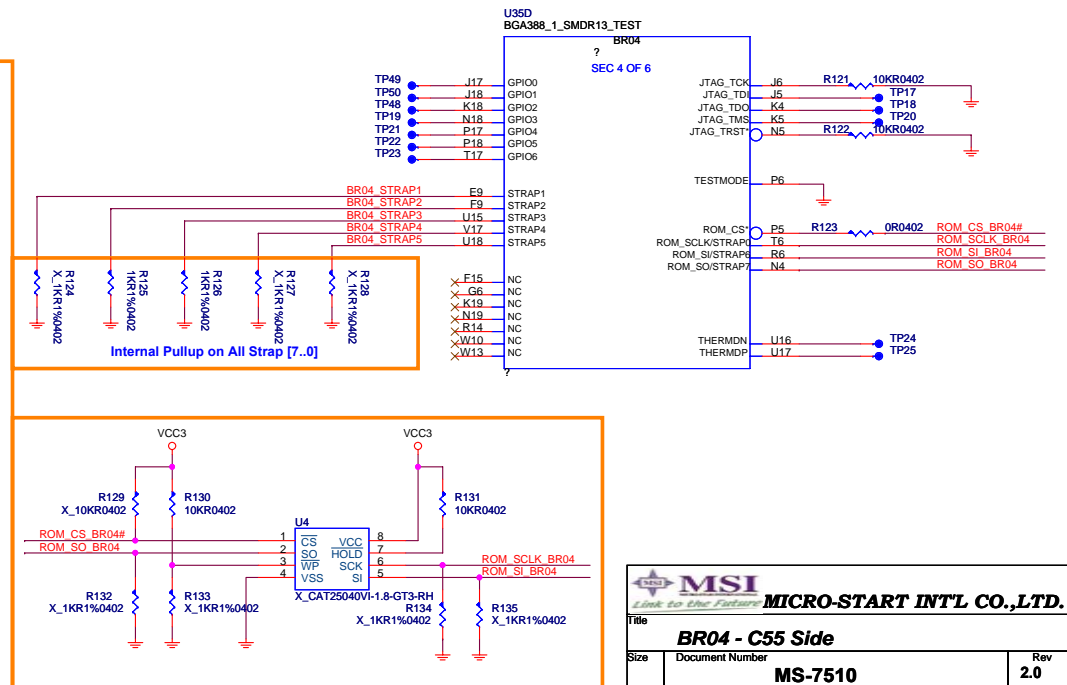
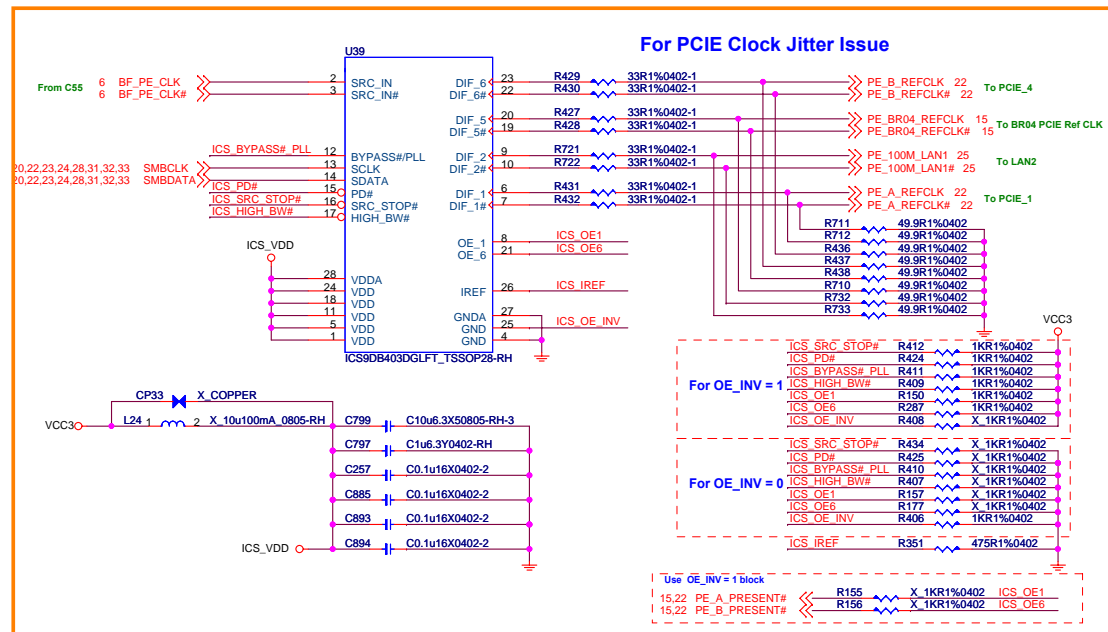
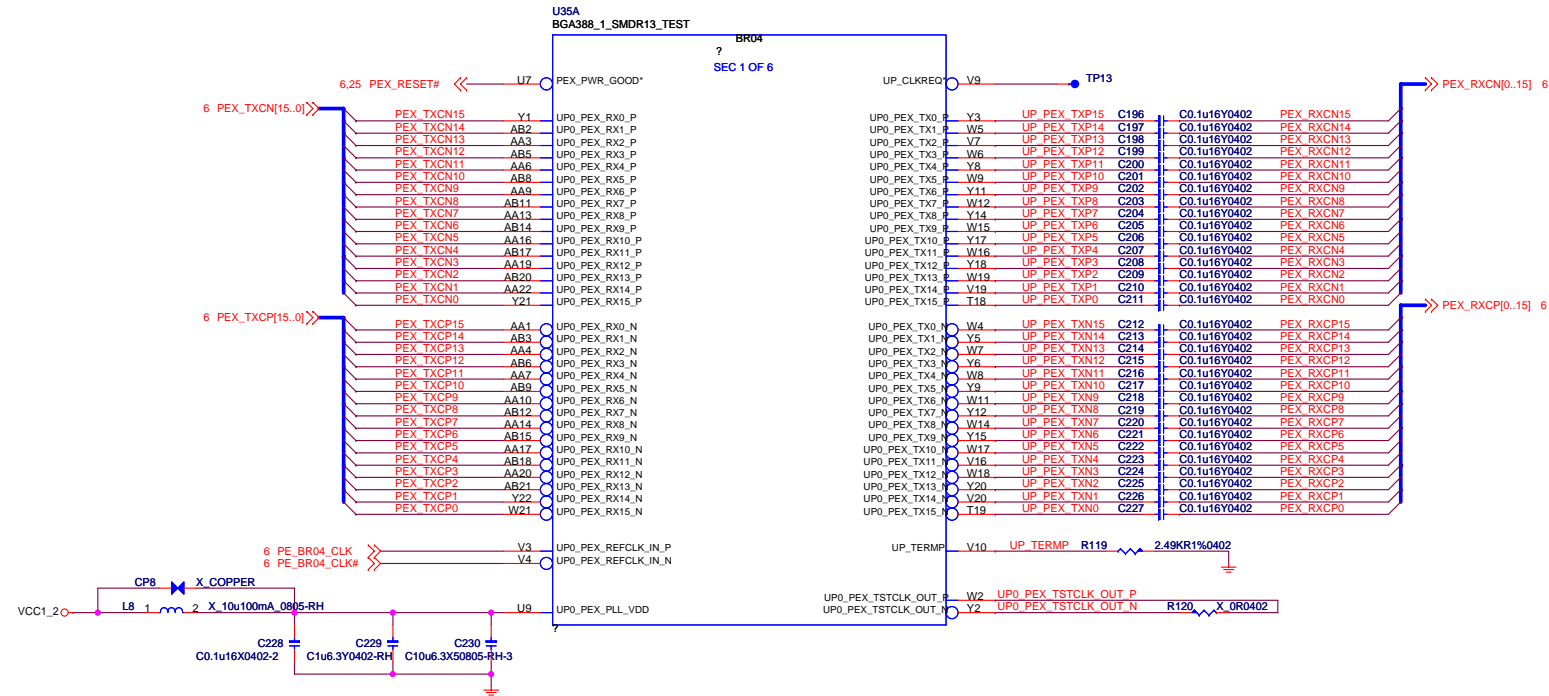
DDR Channel A VCC_DDR Decoupling Caps.



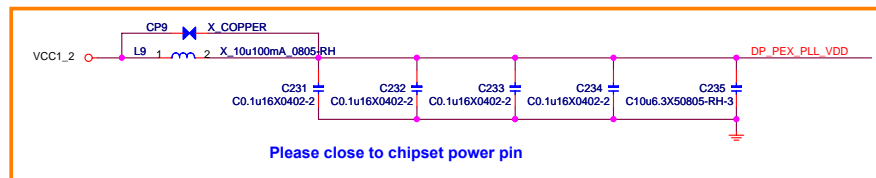
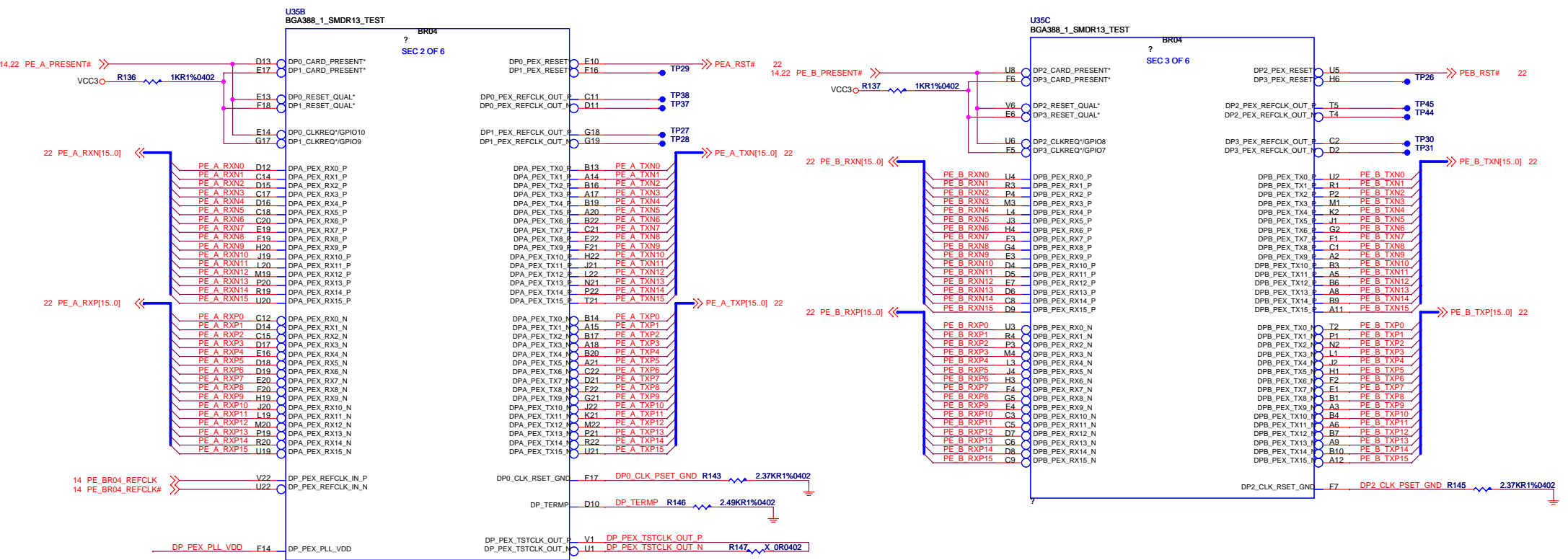
EMI Solution 2007-10-25



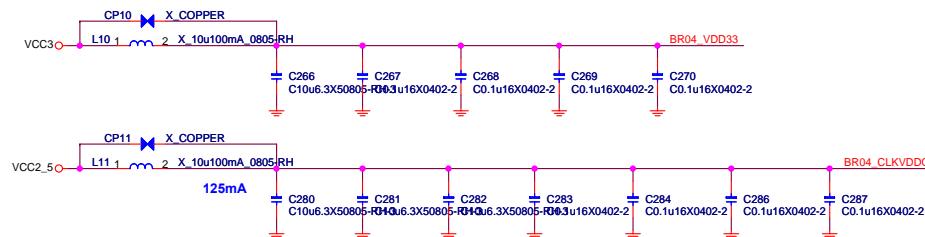
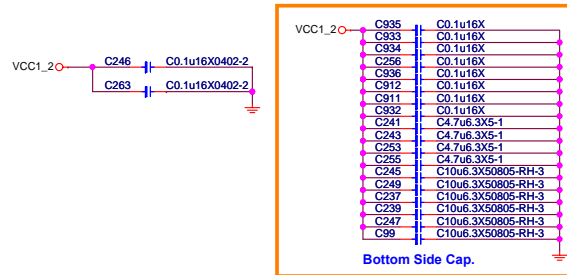
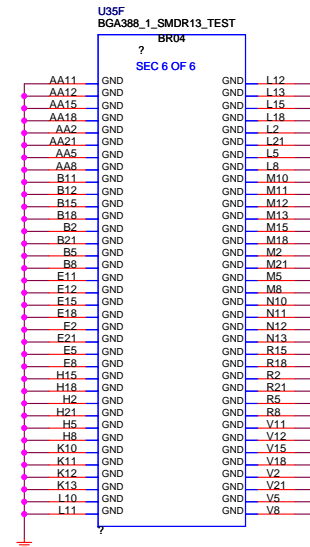
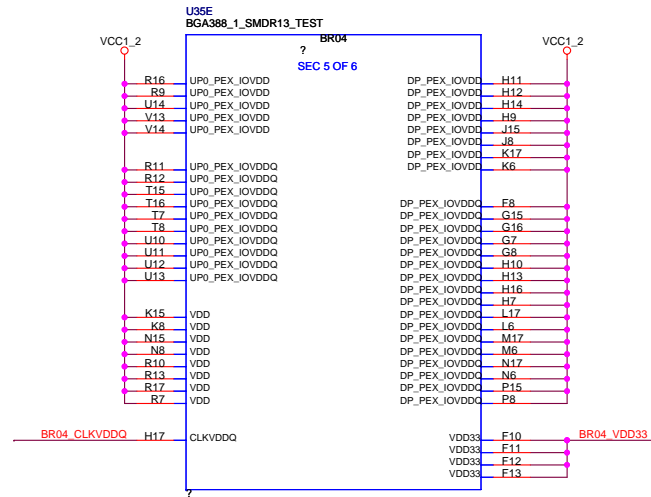
C55 to BR04 PCI-Express Interface



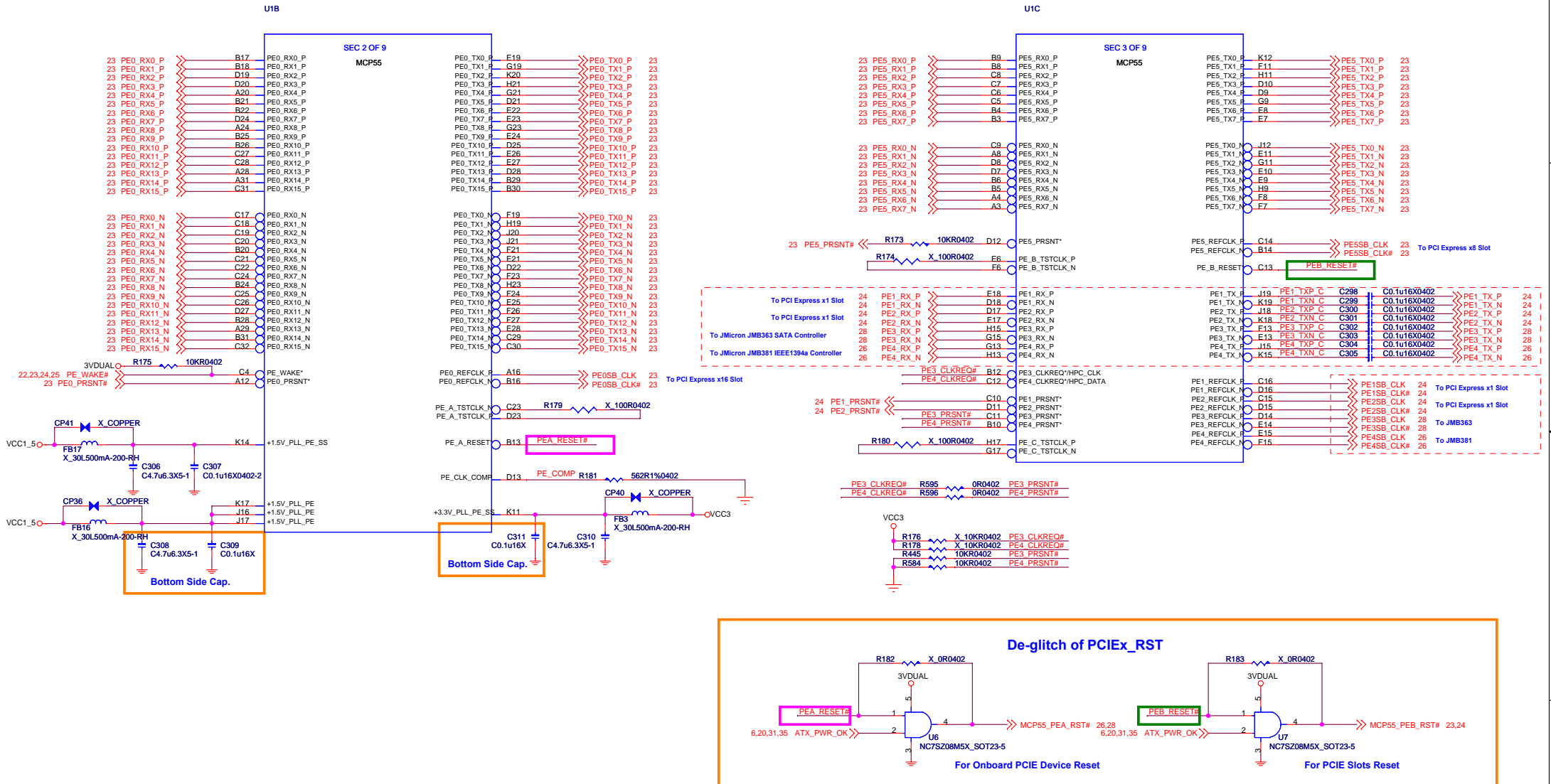
BR04 to PCI-Express Slots

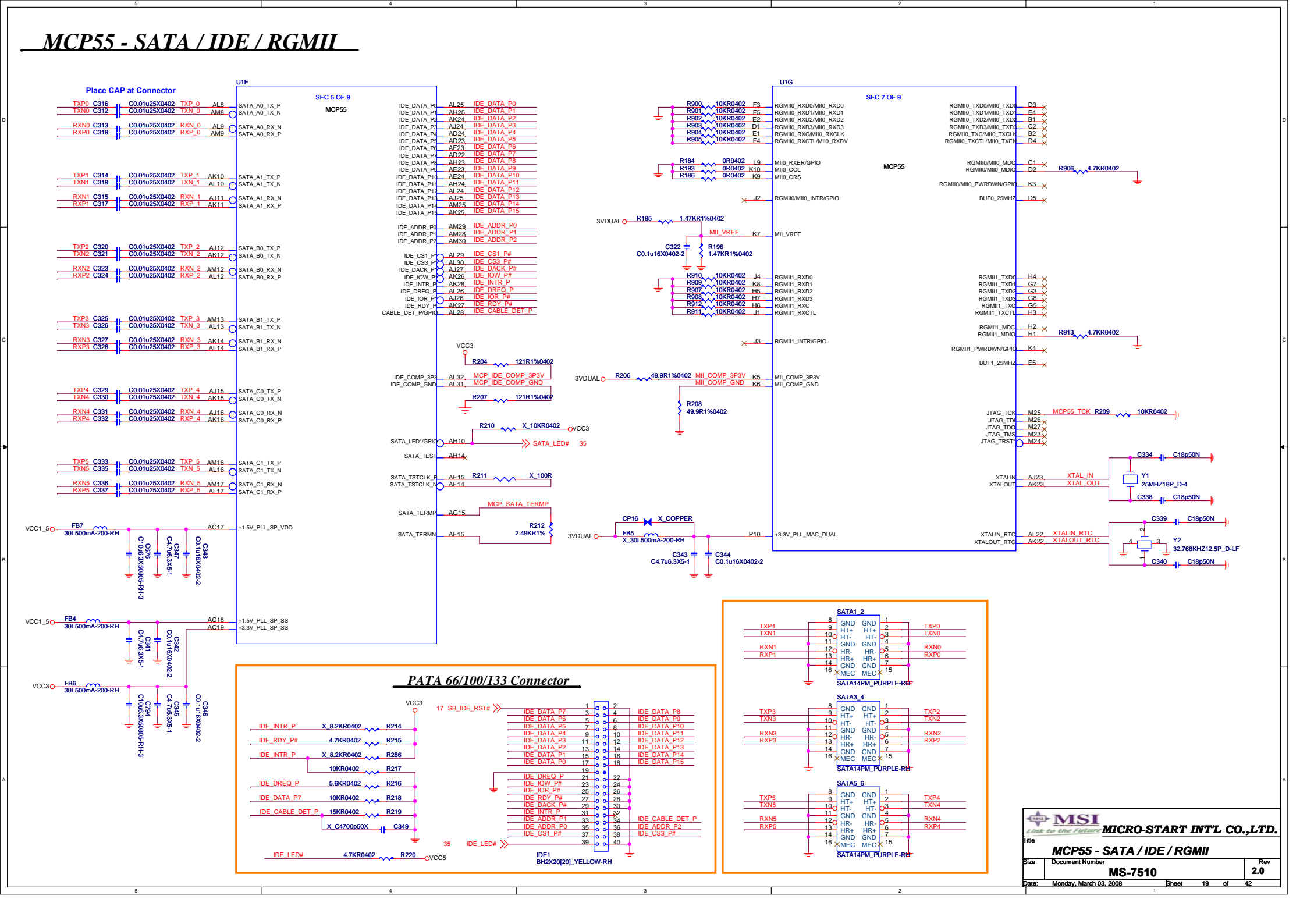
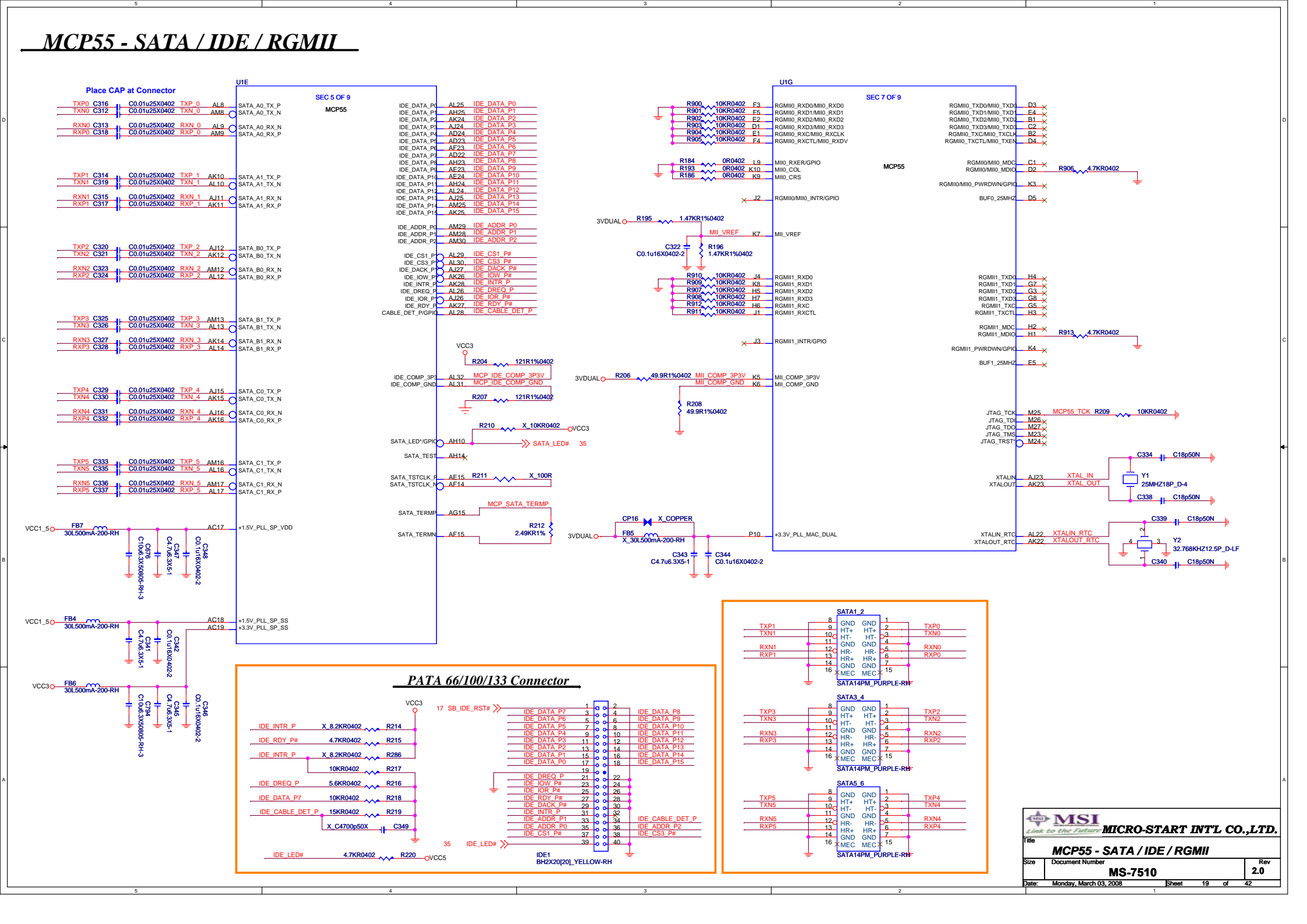


BR04 Power and Gnd Block

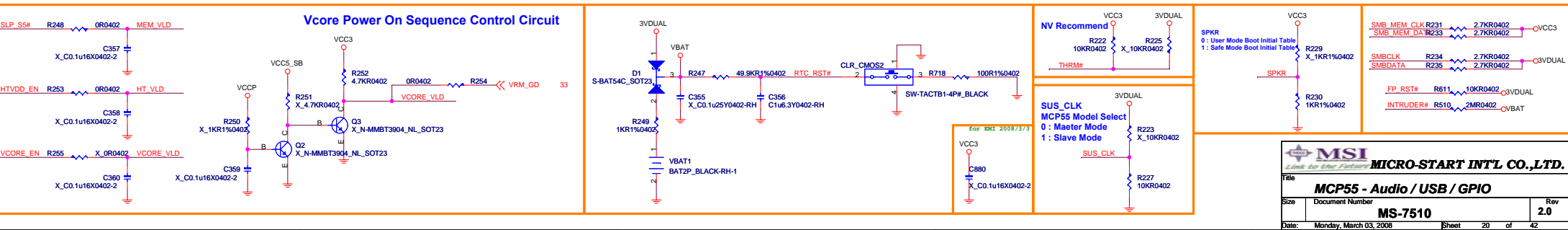
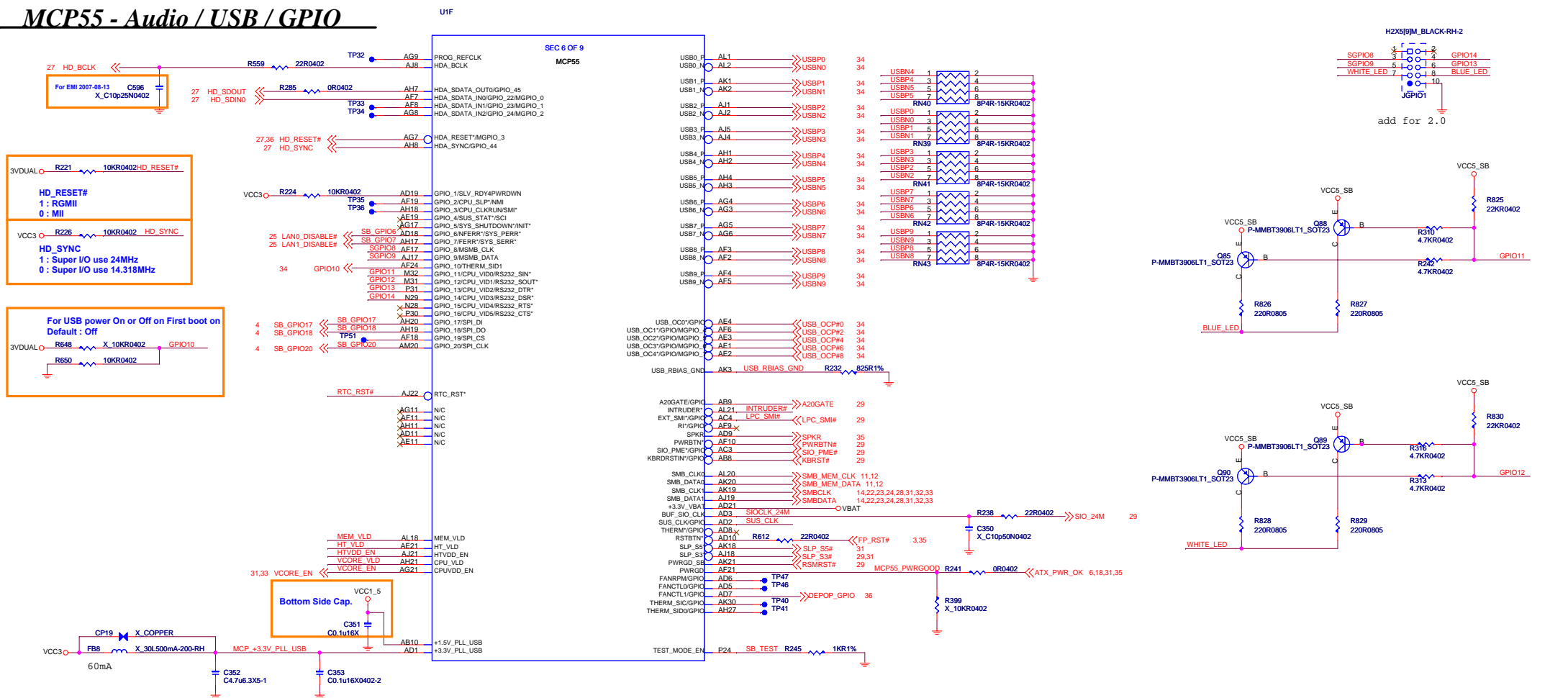


MCP55 - PCI-E

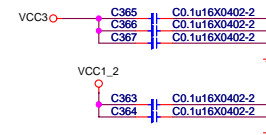
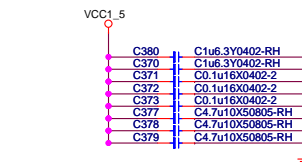
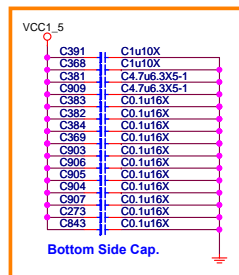
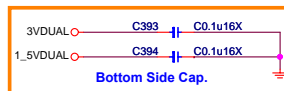
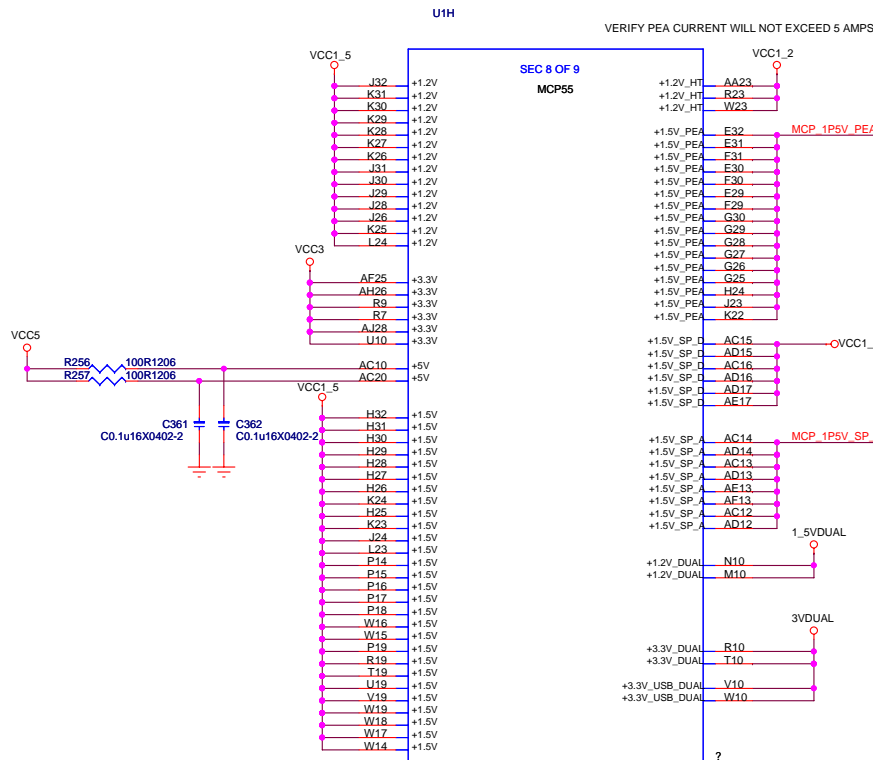
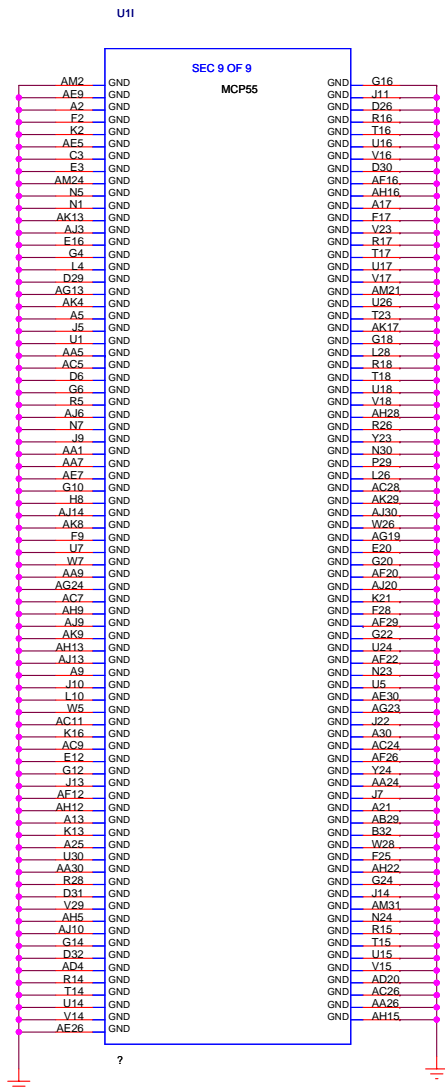


[illegible]

MCP55 - Audio / USB / GPIO

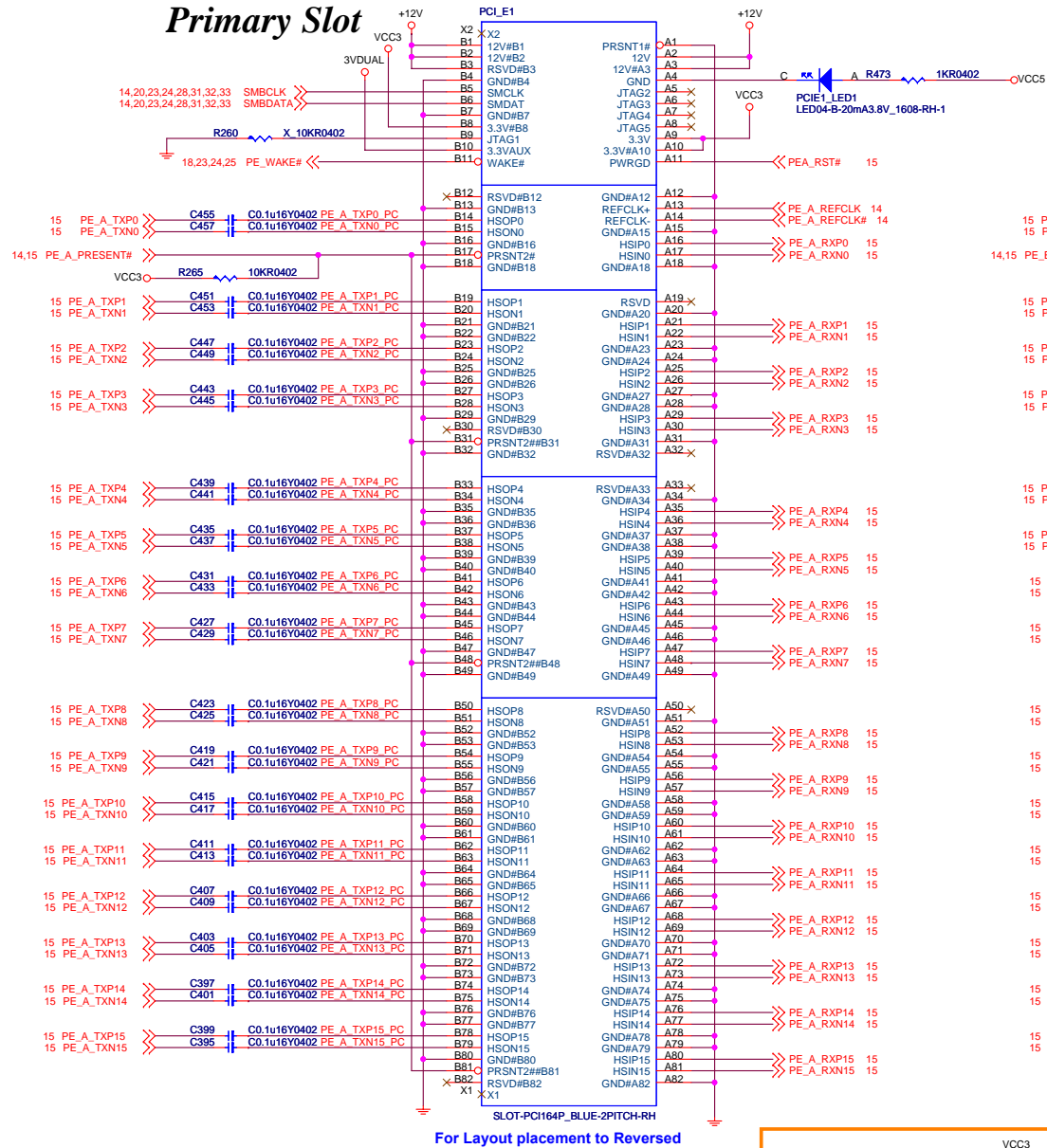


MCP55 - Power & Gnd

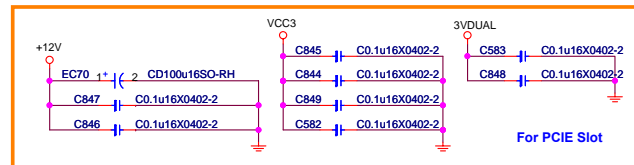
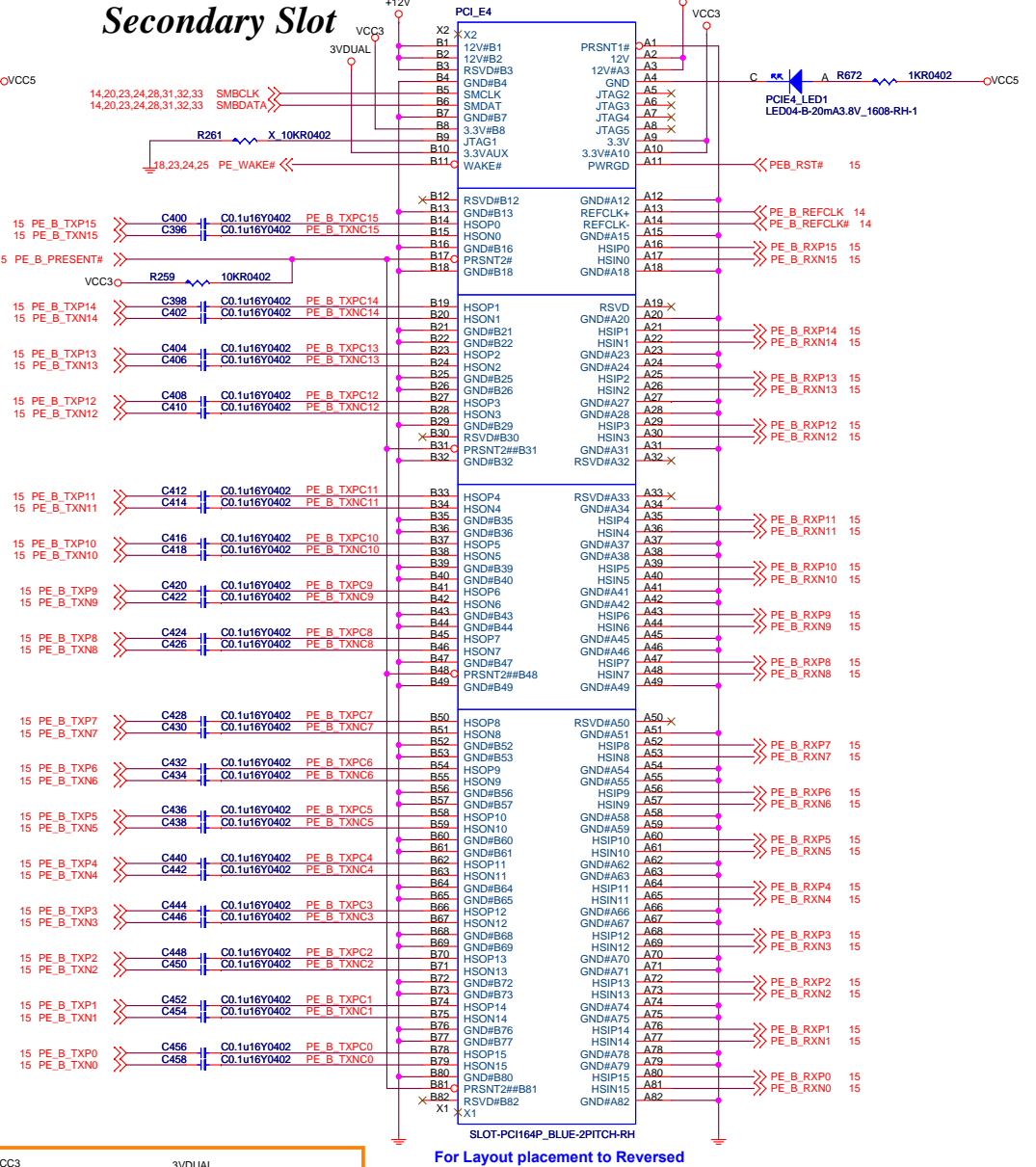


PCI-Express x16 Primary and Secondary Slot

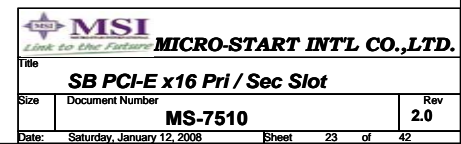
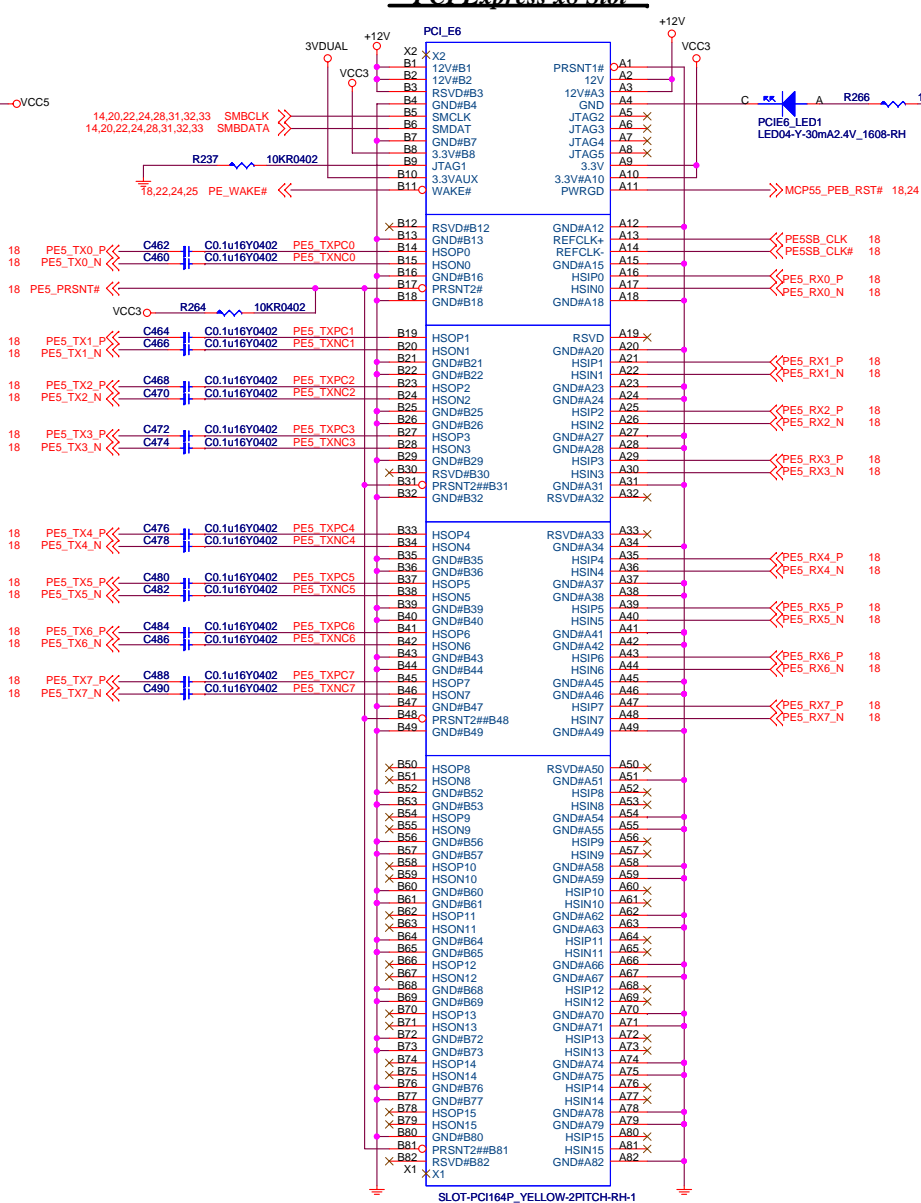
Primary Slot



Secondary Slot

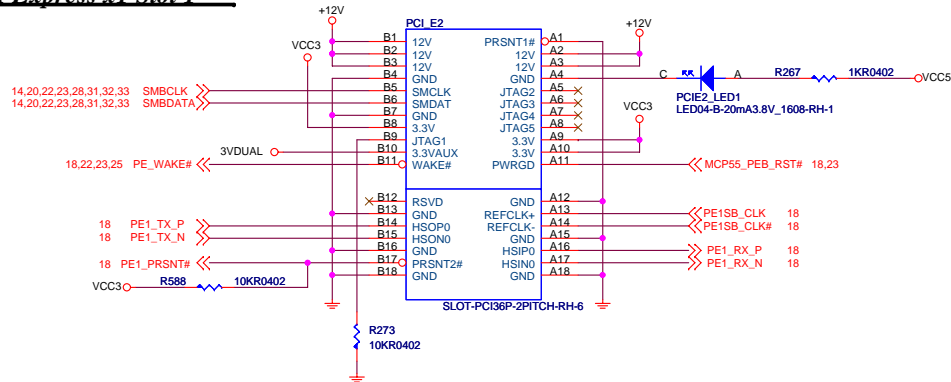


PCI Express x8 Slot

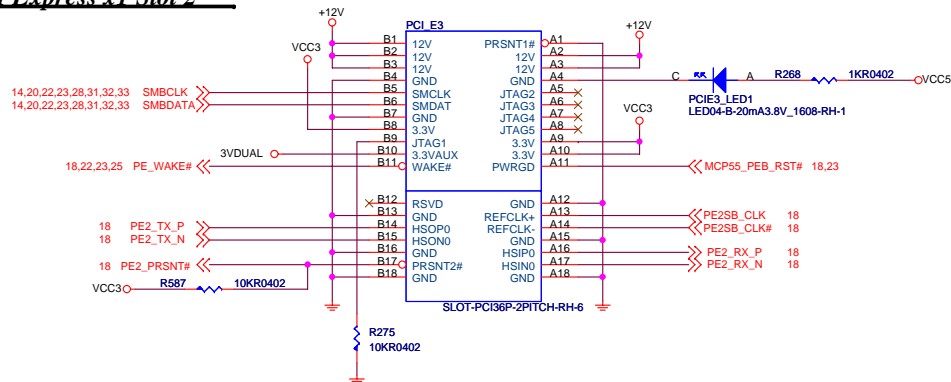


SB PCI-Express x1 Slots and PCI Slot

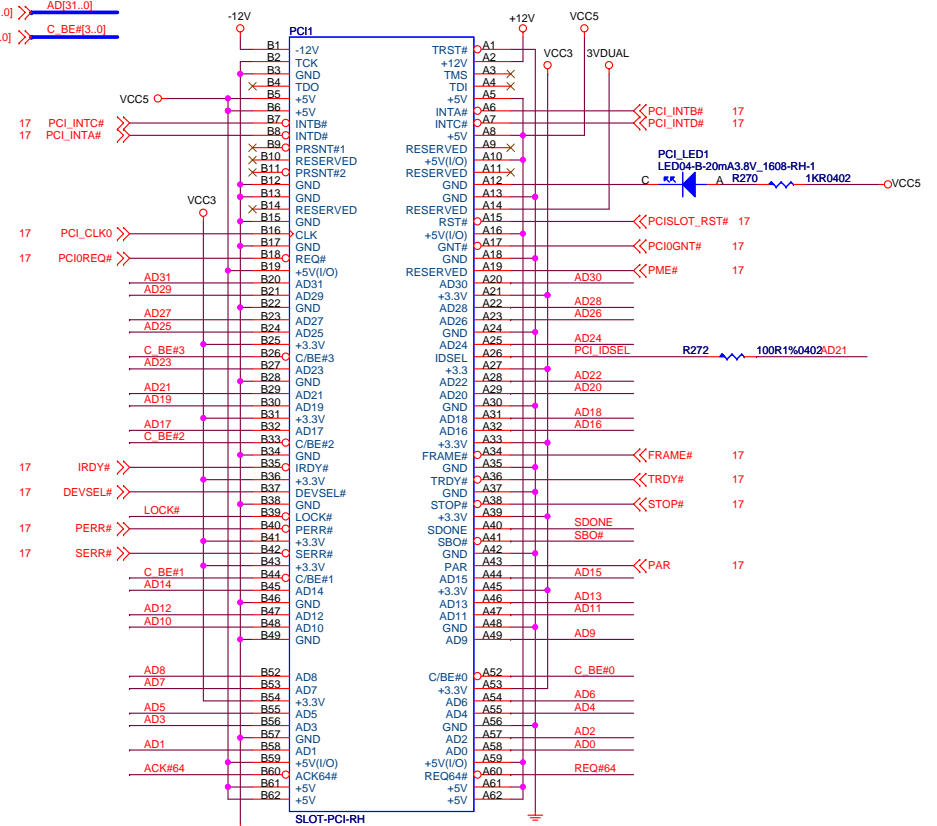
PCI Express x1 Slot 1



PCI Express x1 Slot 2

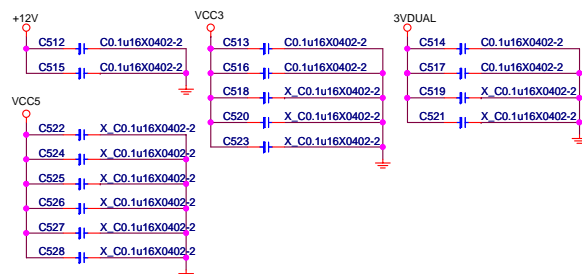


PCI Slot 1 (PCIVER: 2.2 Comply)

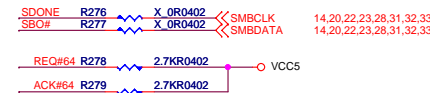
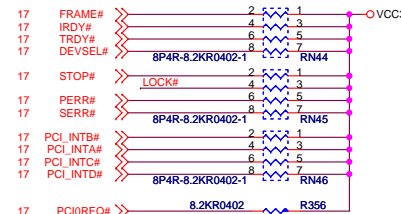


IDSEL = AD21
MASTER = PCI0REQ#
PCI0GNT*

PCISlot Decoupling Capacitors

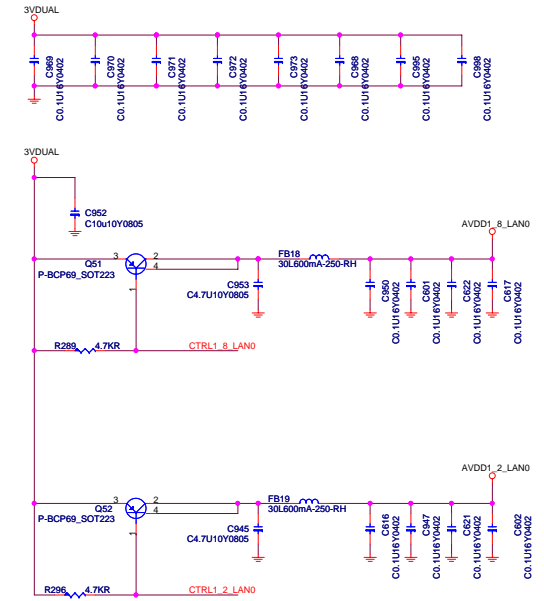
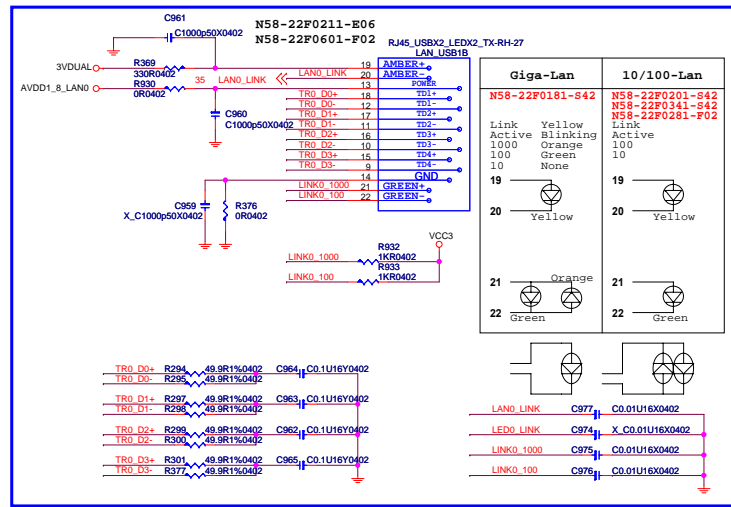
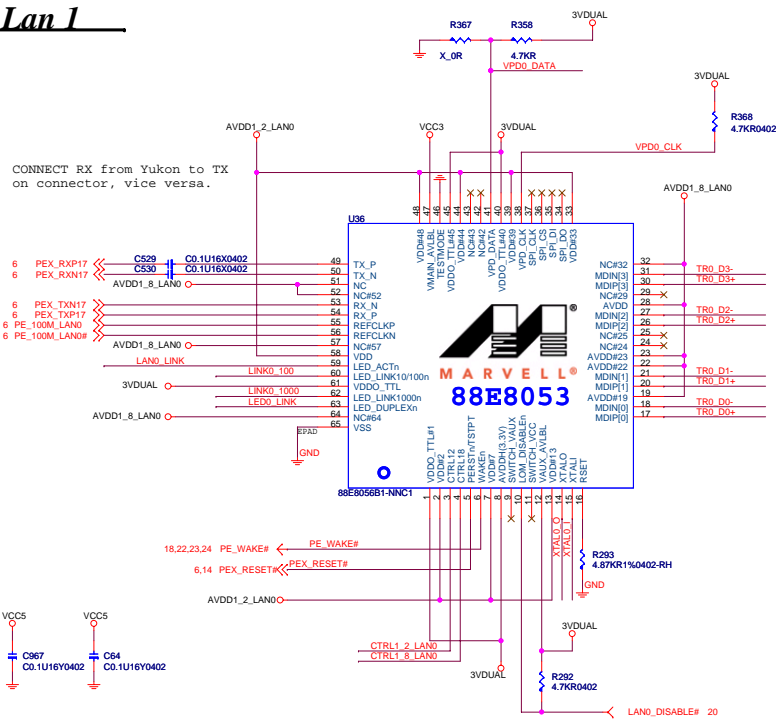


PCI Pull Up / Down Resistors



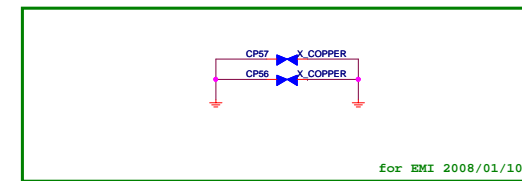
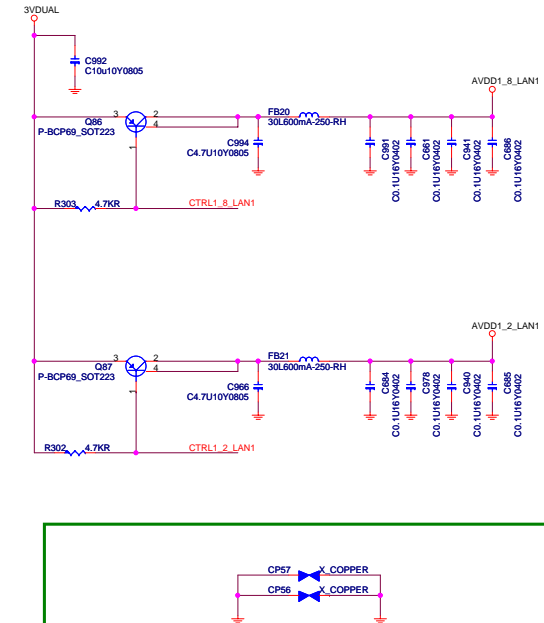
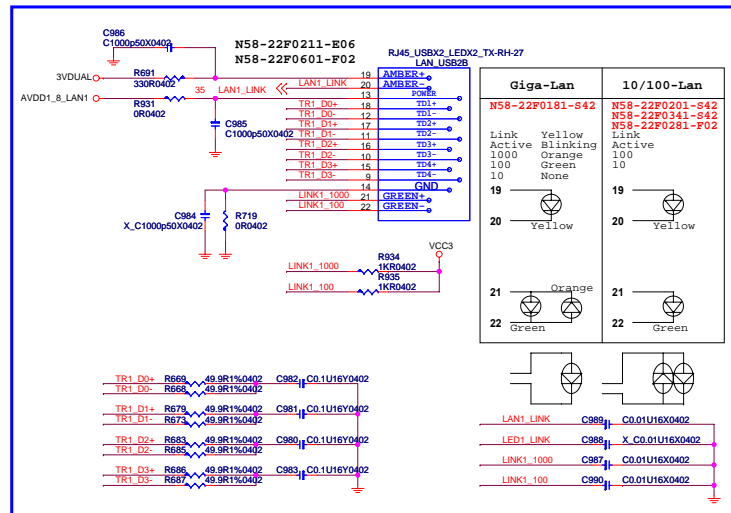
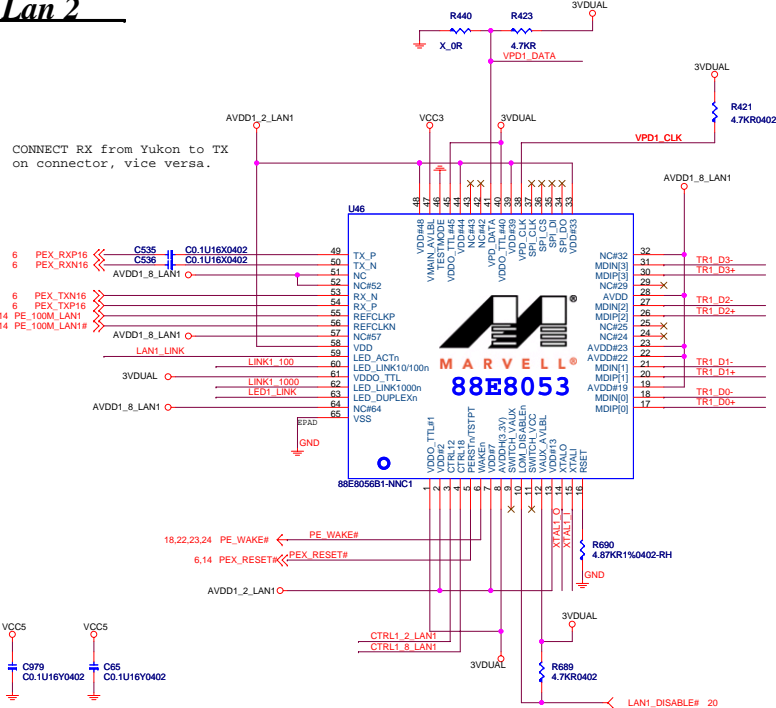
Lan 1

CONNECT RX from Yukon to TX on connector, vice versa.

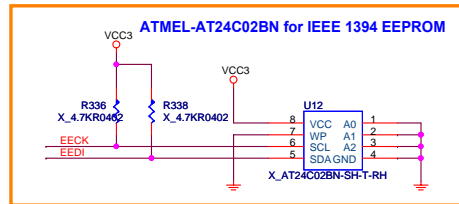
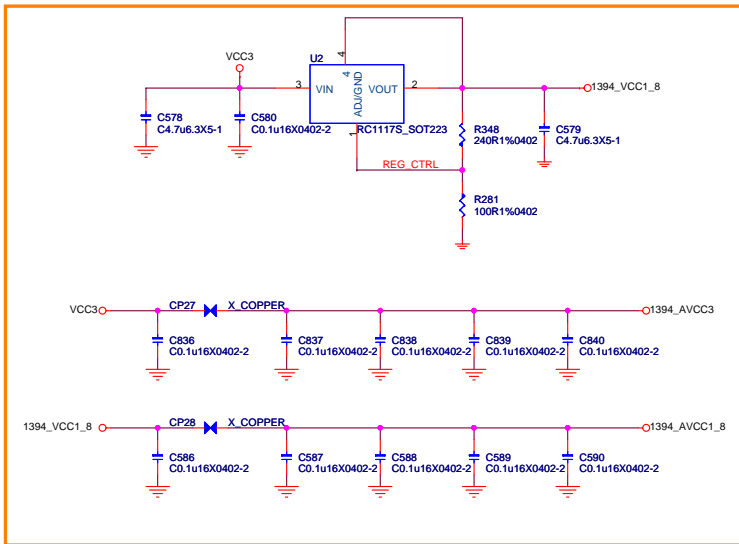
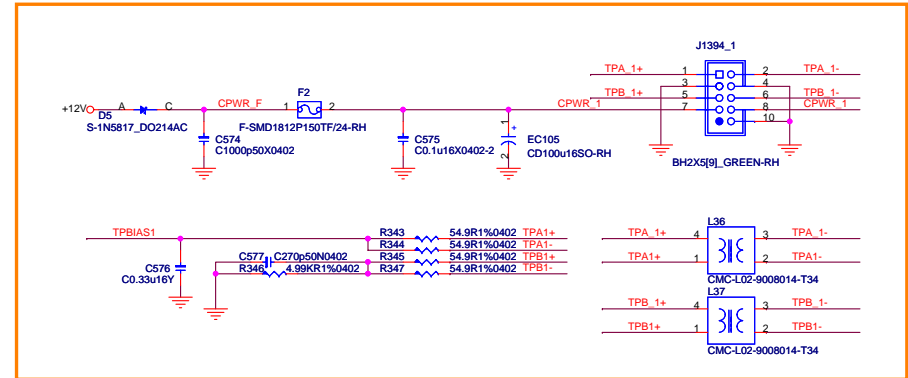
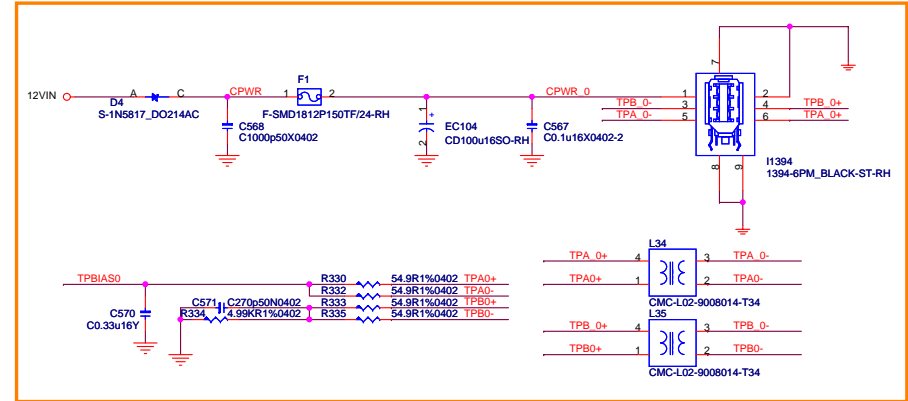
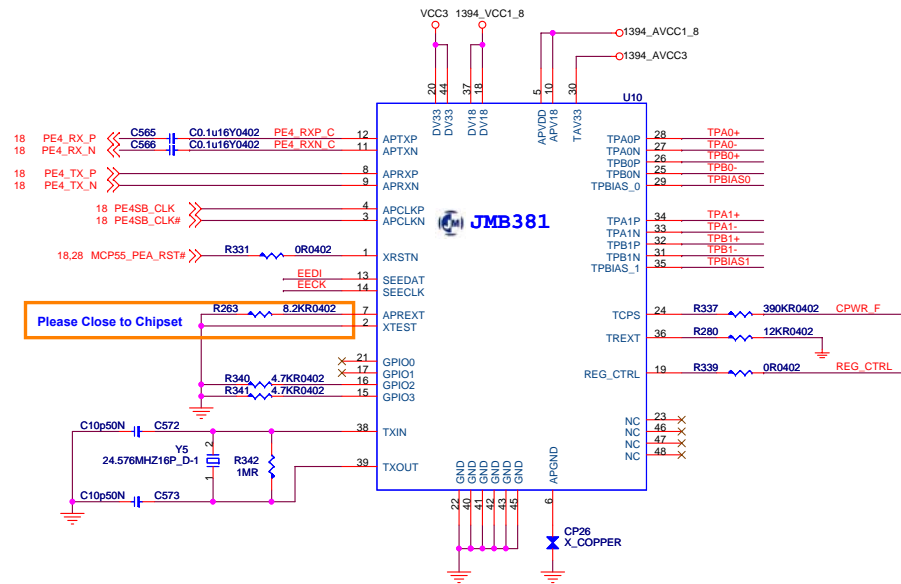


Lan 2

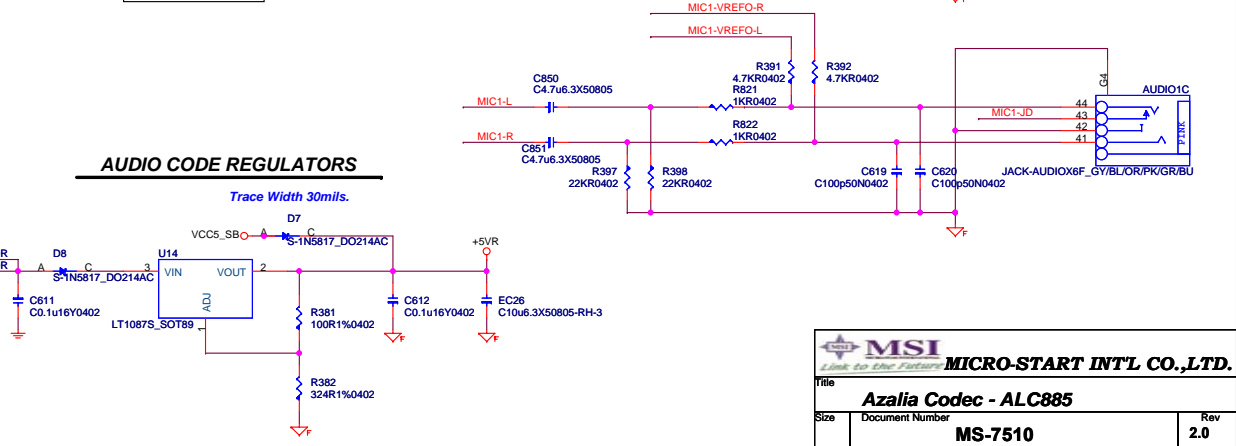
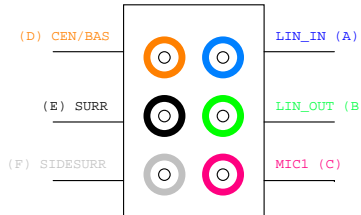
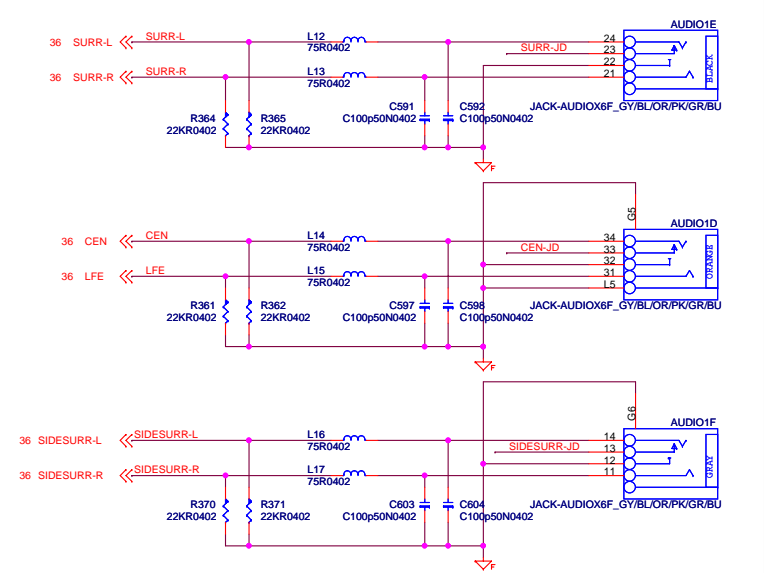
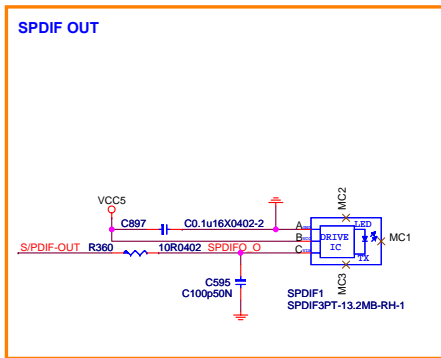
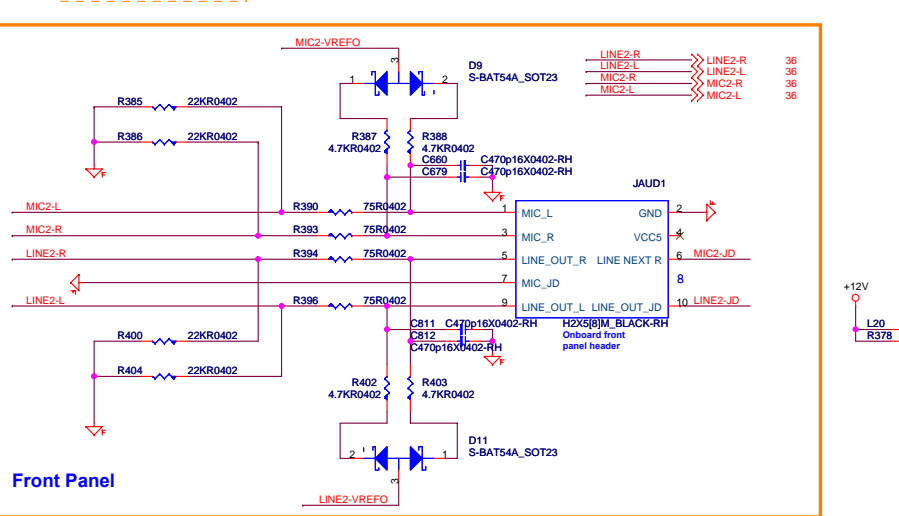
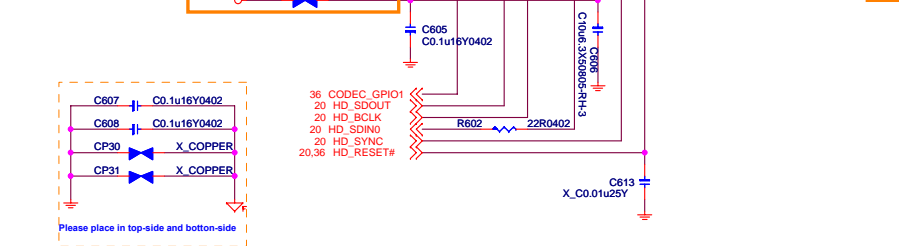
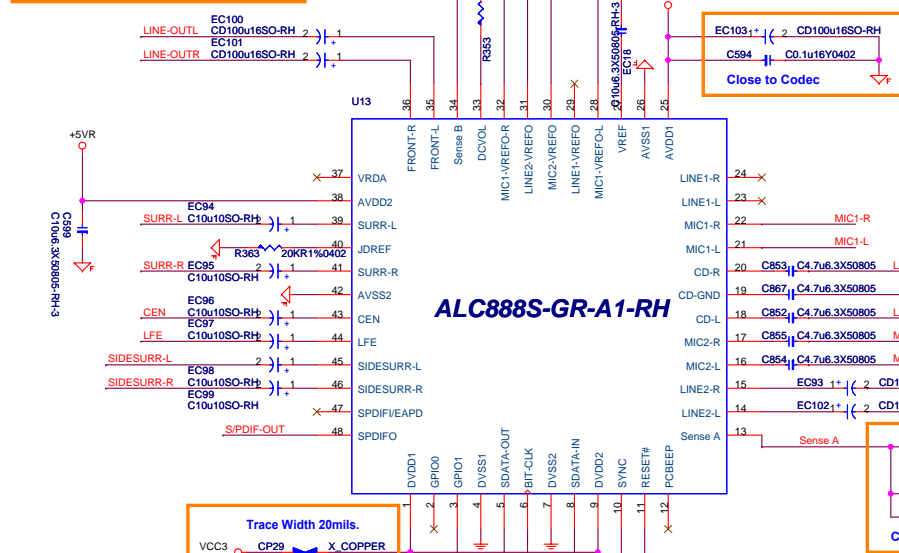
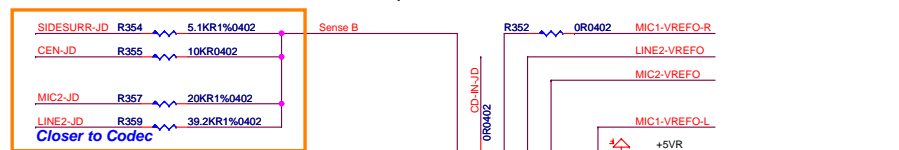
CONNECT RX from Yukon to TX on connector, vice versa.



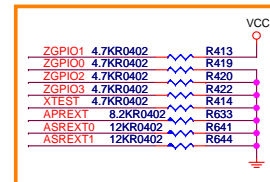
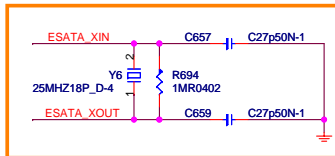
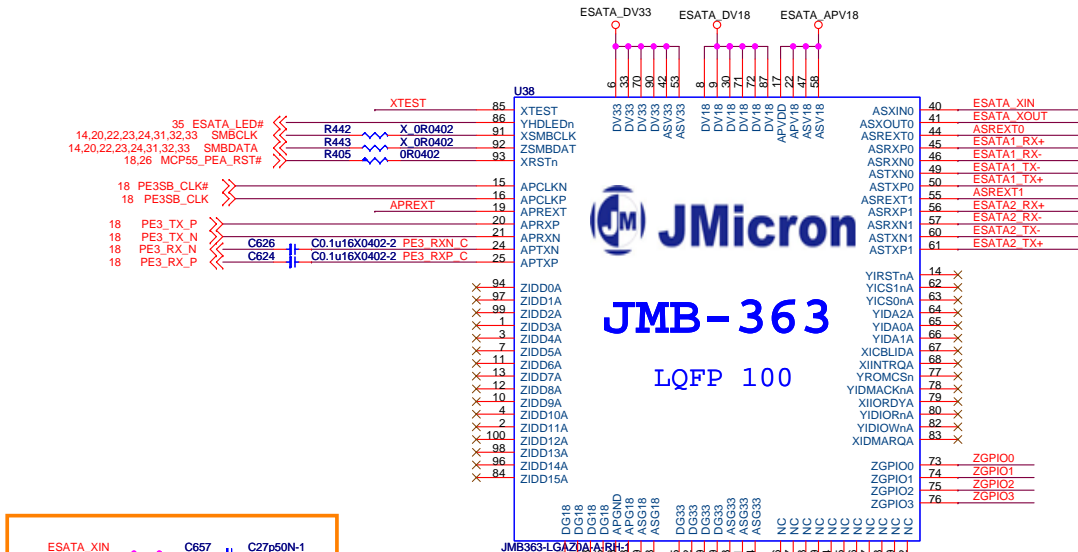
PCIE To 1394a OHCI Host Controller - JMB381



Azalia Codec - ALC888



JMicron JMB363 eSATA Controller



JMB363 GPIO0
It uses to control function# available on JMB363.
0: single function ; 1: multi-function

JMB363 GPIO1
It uses to control clock source of SATA II port 0.
0: from ASXIN0 and ASXOUT0 from PCI Express clock source
1: from ASXIN0 & ASXOUT0

JMB363 GPIO2
It uses to control interface to access internal debug registers.
0: SMBus I/F ; 1: Reserved for debugging.

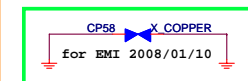
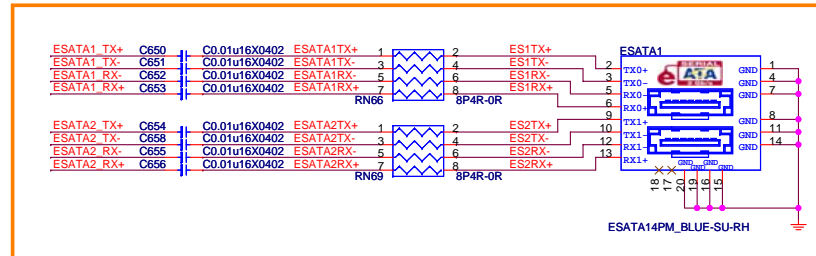
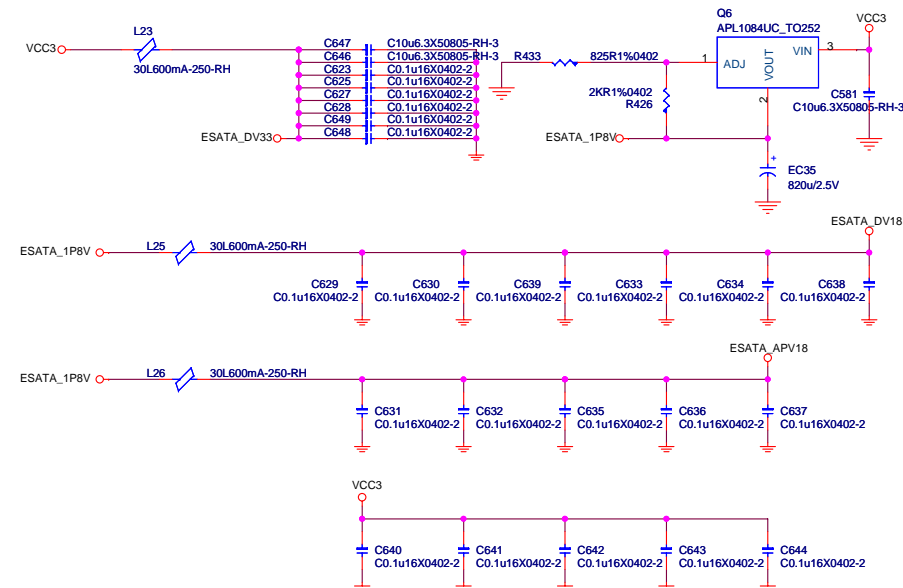
JMB363 GPIO3
Reserved for debugging.

JMB363 Test Mode Enable.
High-active signal to enable testing and debug modes of JMB363.

SATA II Port 0 External Reference Resistor.
An external 12K Ω ±1% resistor should be connected and bypass to the ground ASG18 (pin#48).

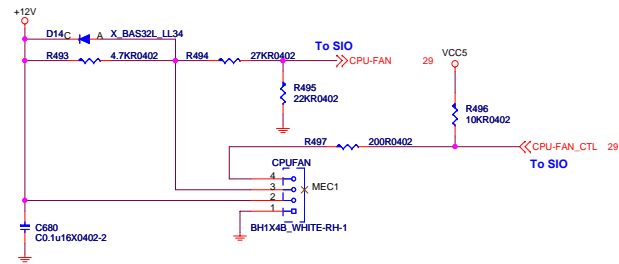
SATA II Port 0 External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground ASG18 (pin#59).

PCI Express External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground APG18 (pin#18)

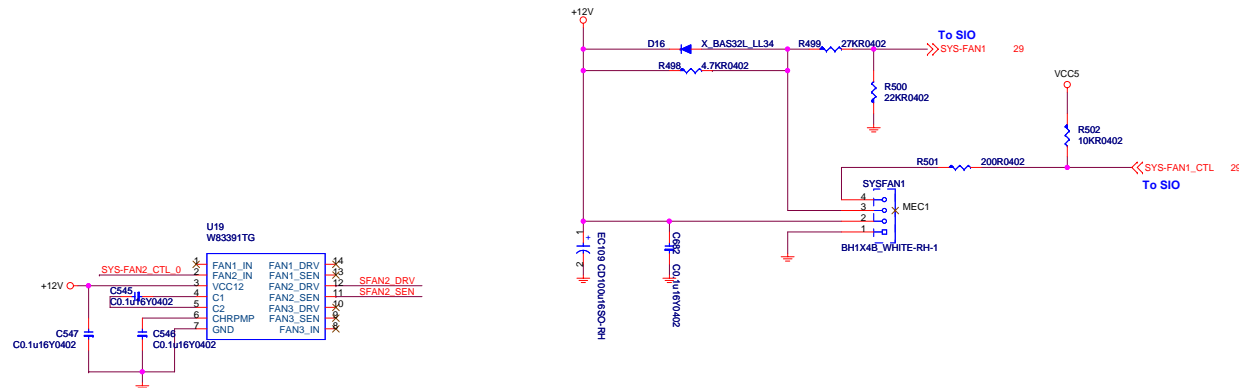


Fan Controller

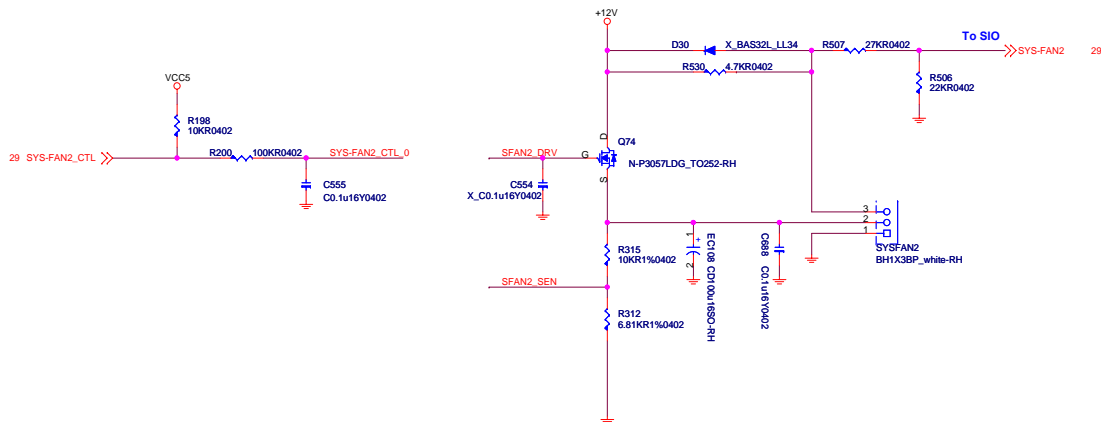
CPU Fan



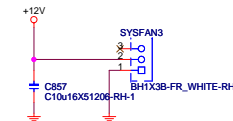
System Fan 1



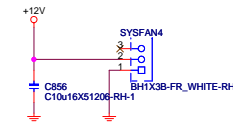
System Fan 2



System Fan 3

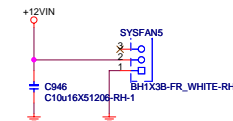


System Fan 4



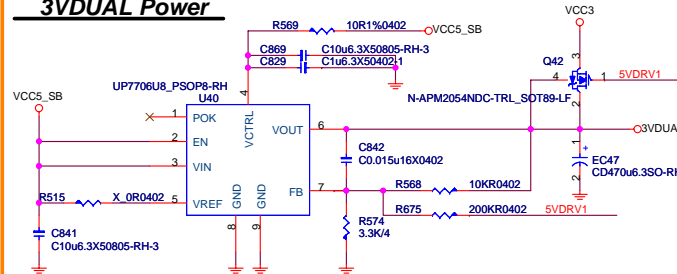
Near the CPU

System Fan 5

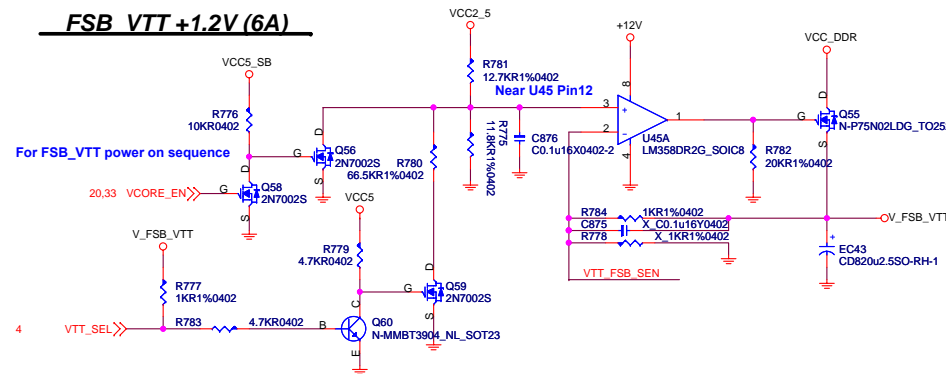


uPLACPI Solution

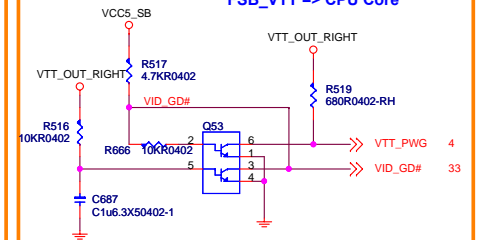
3VDUAL Power



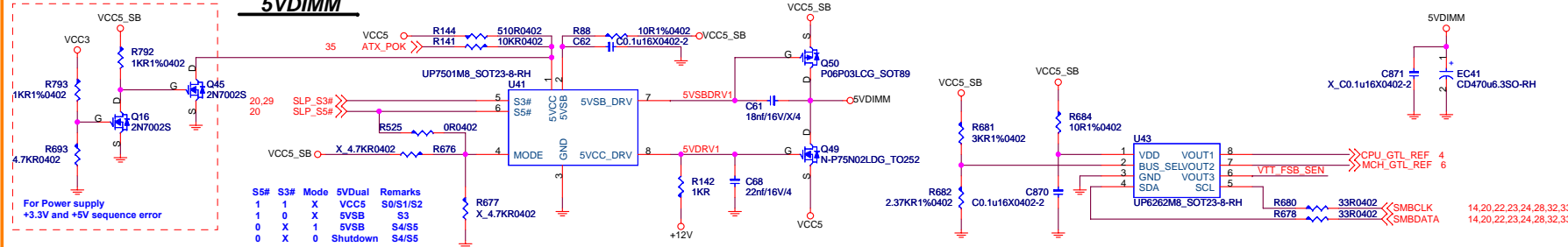
FSB VTT +1.2V (6A)



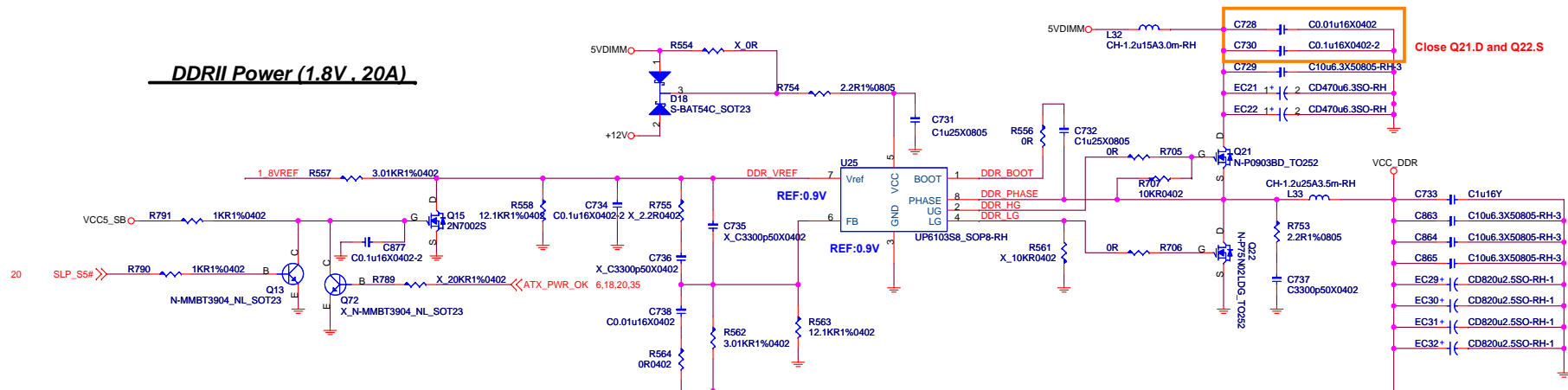
Power on sequence
FSB_VTT => CPU Core



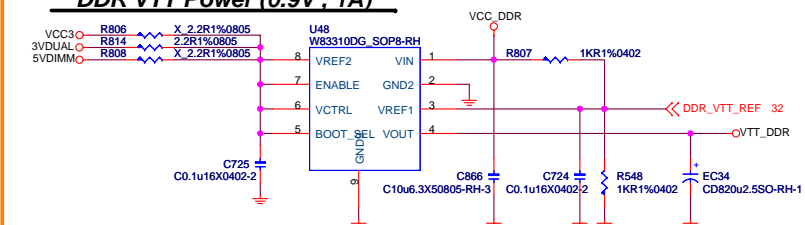
5VDIMM



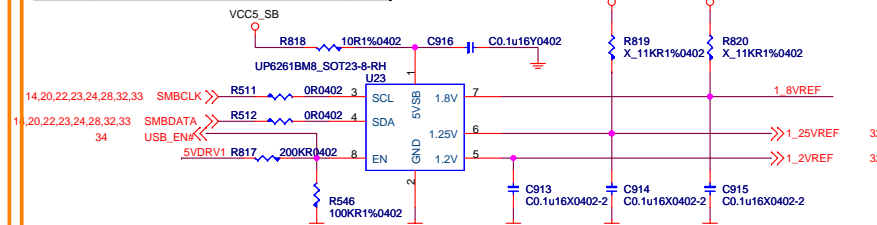
DDRII Power (1.8V, 20A)



DDR VTT Power (0.9V, 1A)



Regulator reference Voltage



MICRO-START INT'L CO.,LTD.

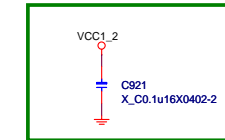
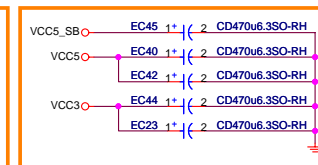
Title	
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MS12 ACPI Controller

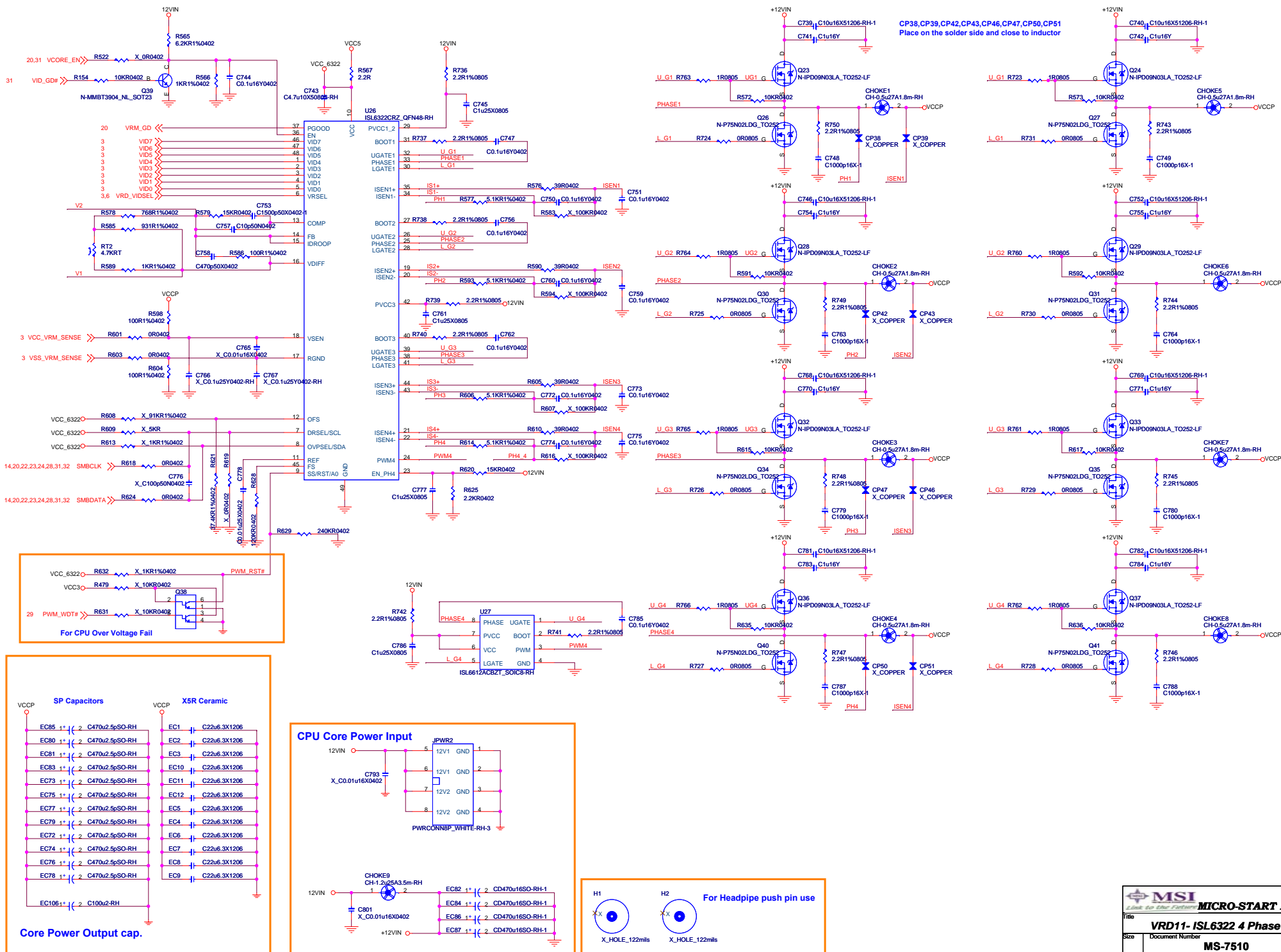
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Size	Document Number	REV
	MS 7510	2.0

C55 + BR04 1.2V Core Power (25A + 10A)

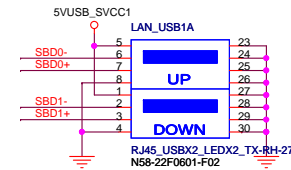
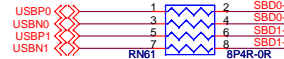
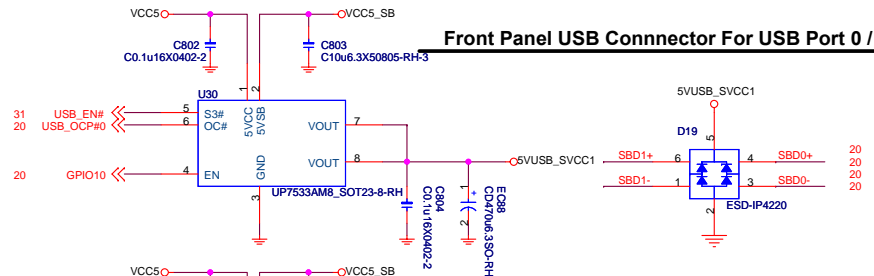
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Voltage Regular Module (VRD11)

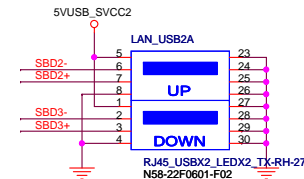
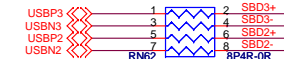
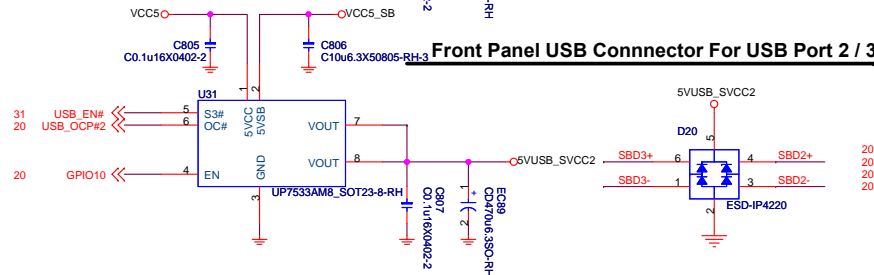


Front Panel and Real I/O USB Connector

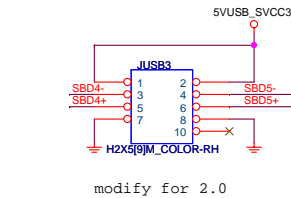
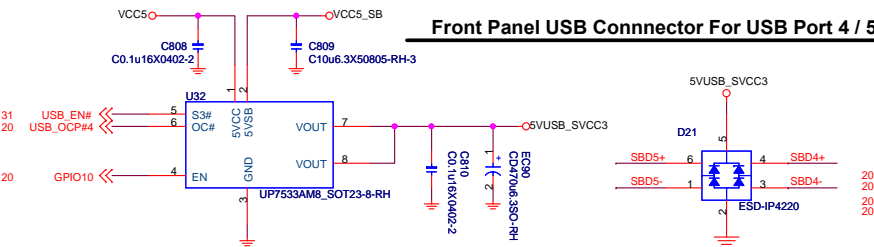
Front Panel USB Connector For USB Port 0 / 1



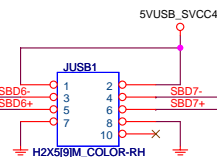
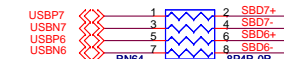
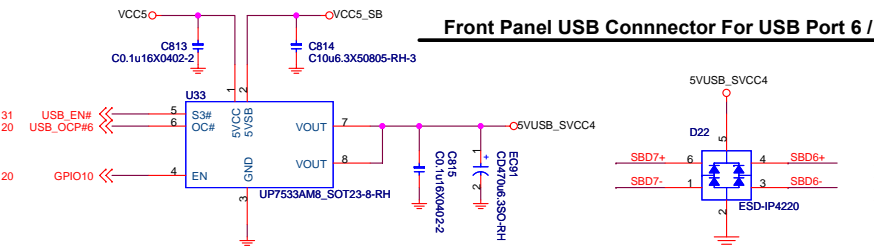
Front Panel USB Connector For USB Port 2 / 3



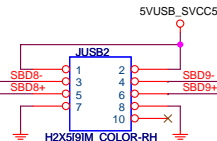
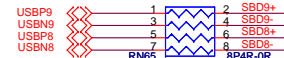
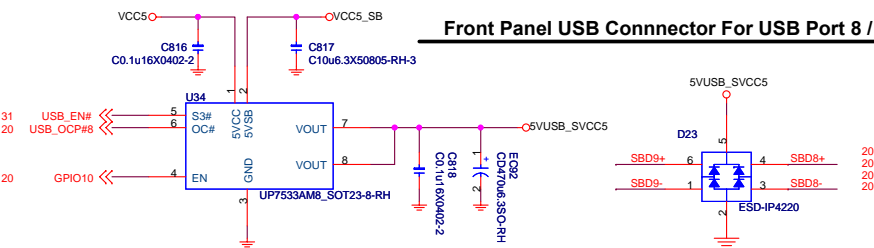
Front Panel USB Connector For USB Port 4 / 5



Front Panel USB Connector For USB Port 6 / 7

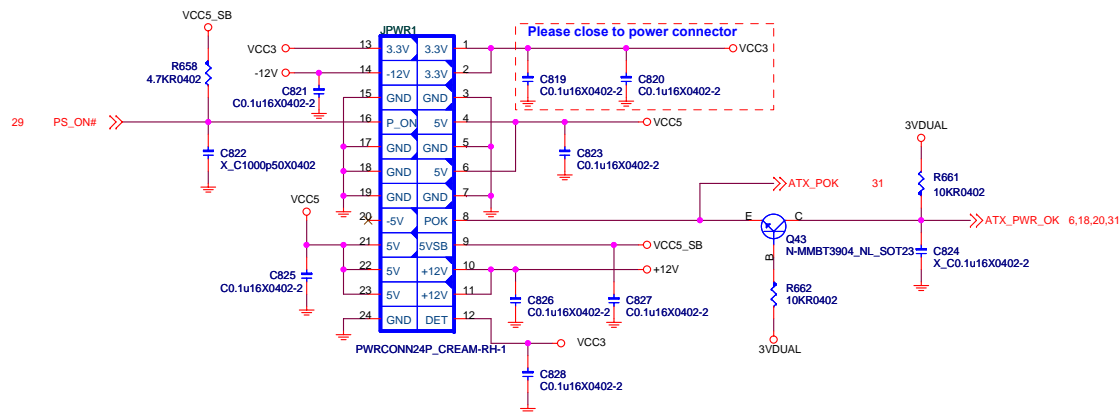


Front Panel USB Connector For USB Port 8 / 9

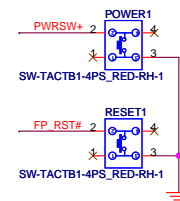


ATX Power Connector / Front Panel / LED

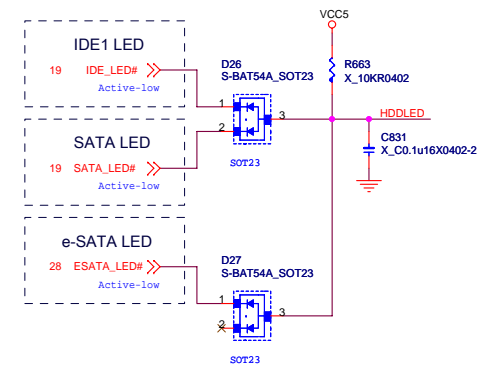
24 Pin ATX Power Connector



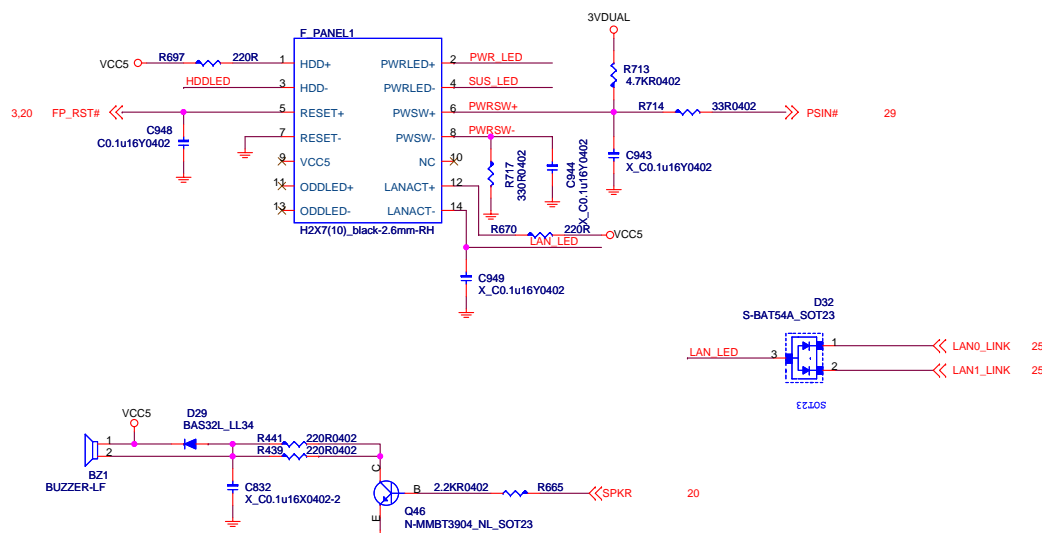
Power and Reset Button



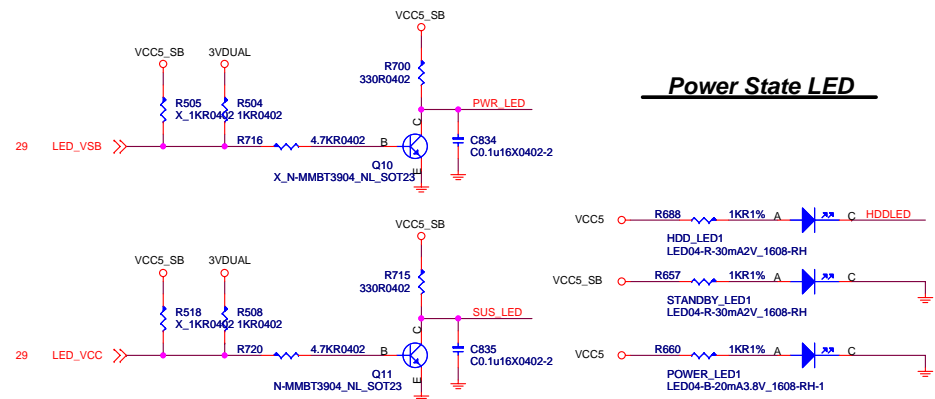
HDD LED



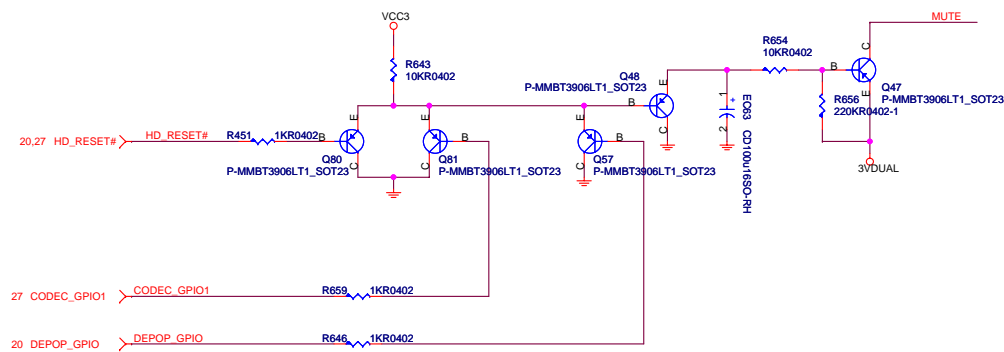
acer Front Panel Connector



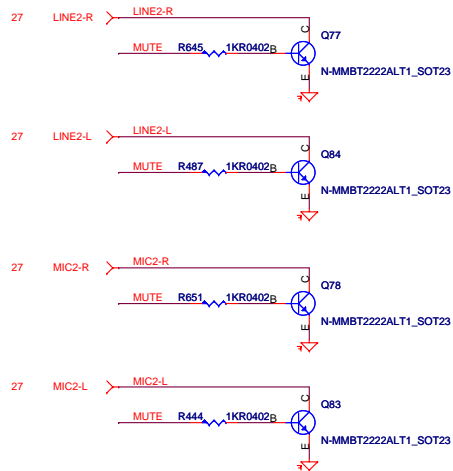
Power State LED



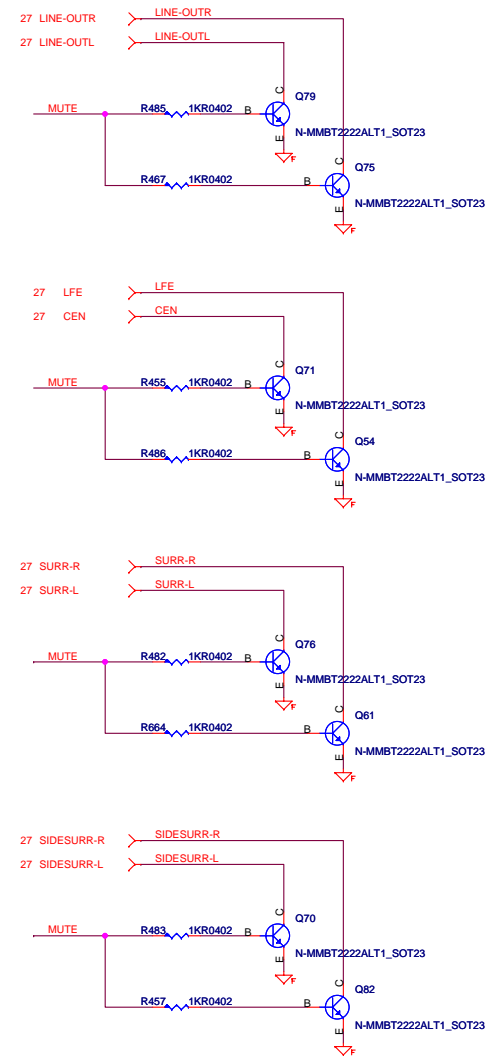
Audio De-Pop Control Circuit

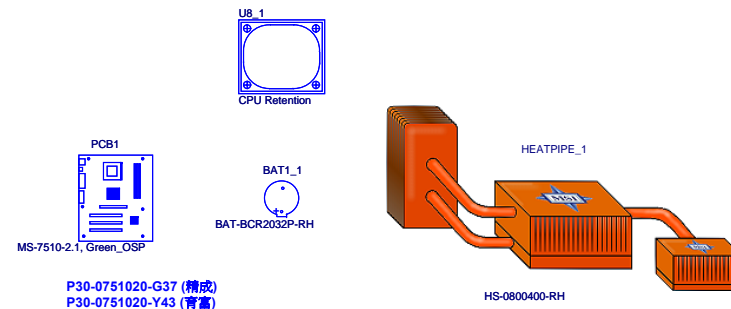
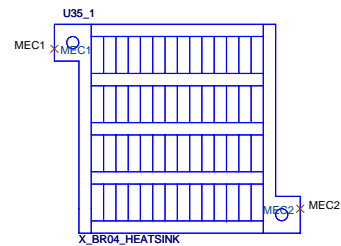
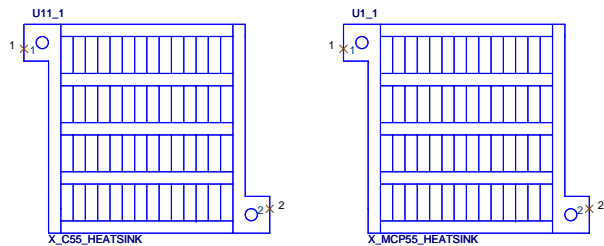


Front Audio Port De-Pop Circuit



Rear Audio Port De-Pop Circuit



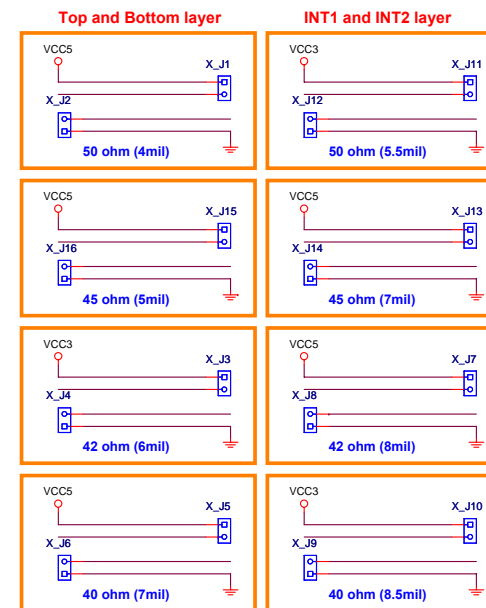
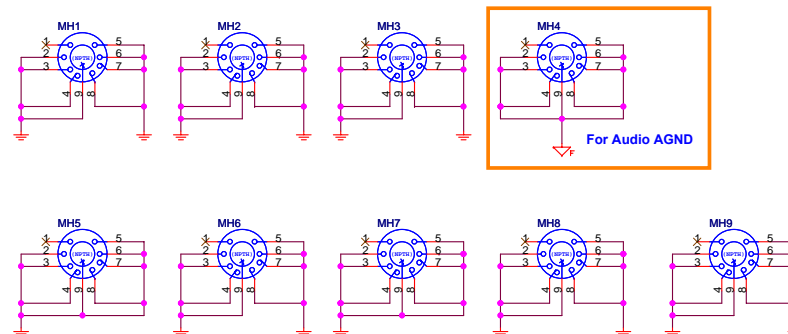
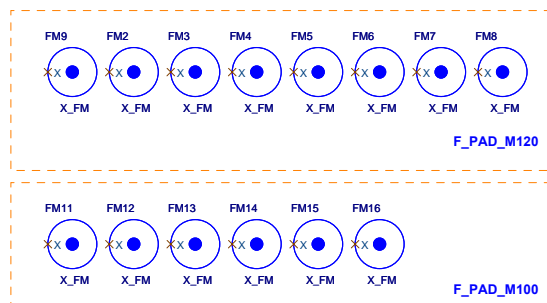


P30-0751020-G37 (精成)
P30-0751020-Y43 (寶富)

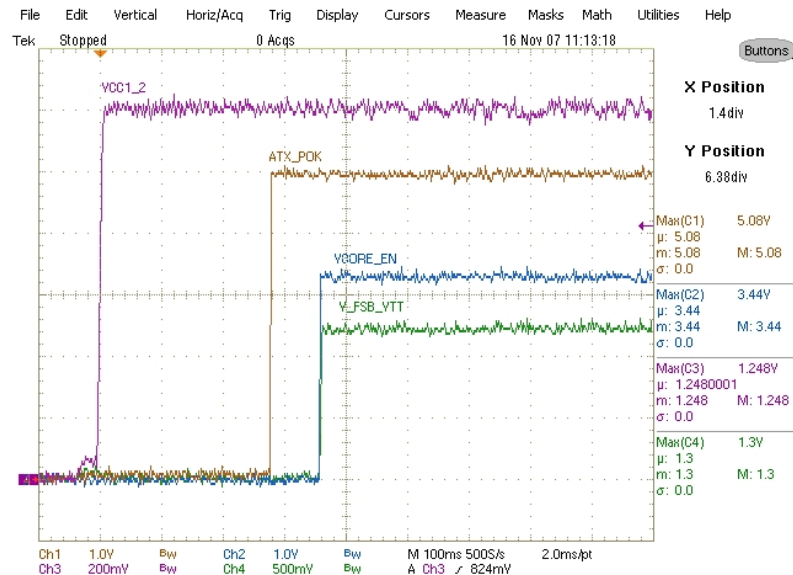
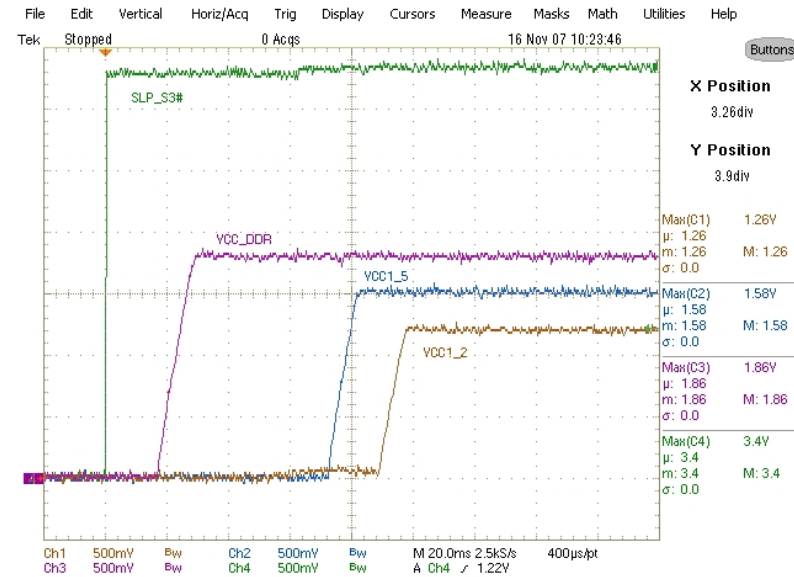
Simulation

Optics Orientation Holes

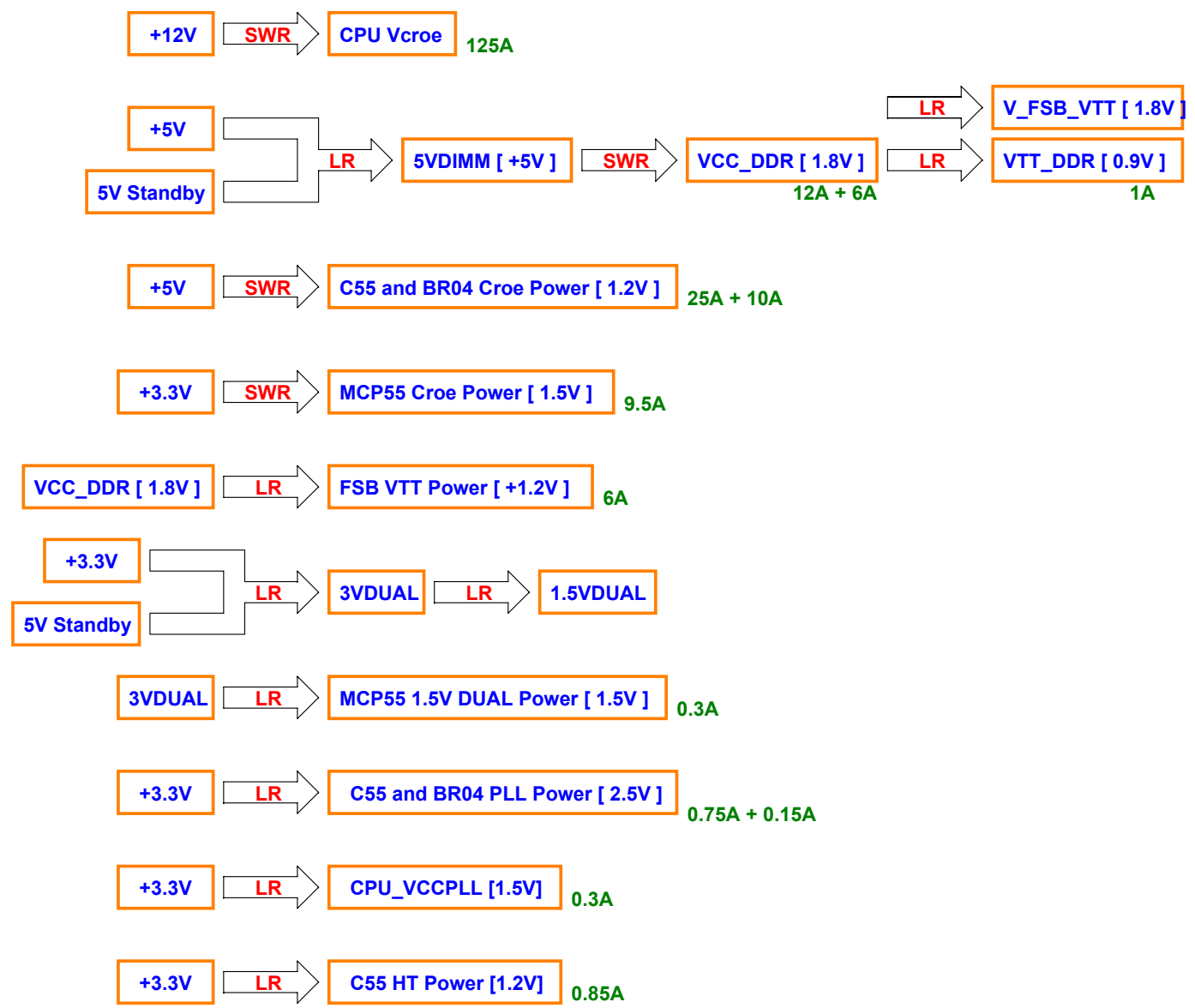
PCB Mounting Holes



Power On/Off Sequence



Syatem Power Map



Configuration & GPIO

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	PCI Reset
PCI slot 1	PIRQ#A	PCIOREQ# PCIOGNT#	AD21	PCI_CLK0	PCISLOT_RST#

DDRII DIMM Configuration

DIMM1	DIMM2	DIMM3	DIMM4
A0 1010000B	A4 1010010B	A2 1010001B	A6 1010011B
0A	0B	1A	1B

SMBus Distribution

SMBus	Power	Load
SMBDATA SMBCLK	VCC3	MCP55 , JM363 , PWM , Super I/O , uPI Power IC PCI Express x16 Slot * 3 , PCI Express x 8 Slot * 1 , PCI Express x 1 Slot * 1 , PCI Slot
SMB_MEM_DATA SMB_MEM_CLK	VCC3_SB	MCP55

System Reset Signal

Signal	Device
PE_RESET#	BR04
H_CPURST#	CPU
HTMCP_RST#	C55
PE_A_RESET#	BR04 PCI Express x 16 Primary Slot
PE_B_RESET#	BR04 PCI Express x 16 Secondary Slot
PEA_RESET#	JMicron JMB363 eSATA Controller JMicron JMB381 IEEE 1394a Host Controller
PEB_RESET#	MCP55 PCI Express x 16 Slot MCP55 PCI Express x 8 Slot MCP55 PCI Express x 1 Slot
PCISLOT_RST#	MCP55 PCI Slot
C55_PCIRST#	C55
SB_IDE_RST#	Master IDE Connector
SIO_RST#	Super I/O
PEX_RESET#	LAN1_MARVELL/88E8056
PEX_RESET#	LAN2_MARVELL/88E8056

SuperI/O GPIO Function

Pin Name	Function Description
GP4	CPU_GTL_REF Select
GP5	Reset PWM
SLOT0CC#	Detect CPU remove or not
COPEN#	Detect Case Open or not

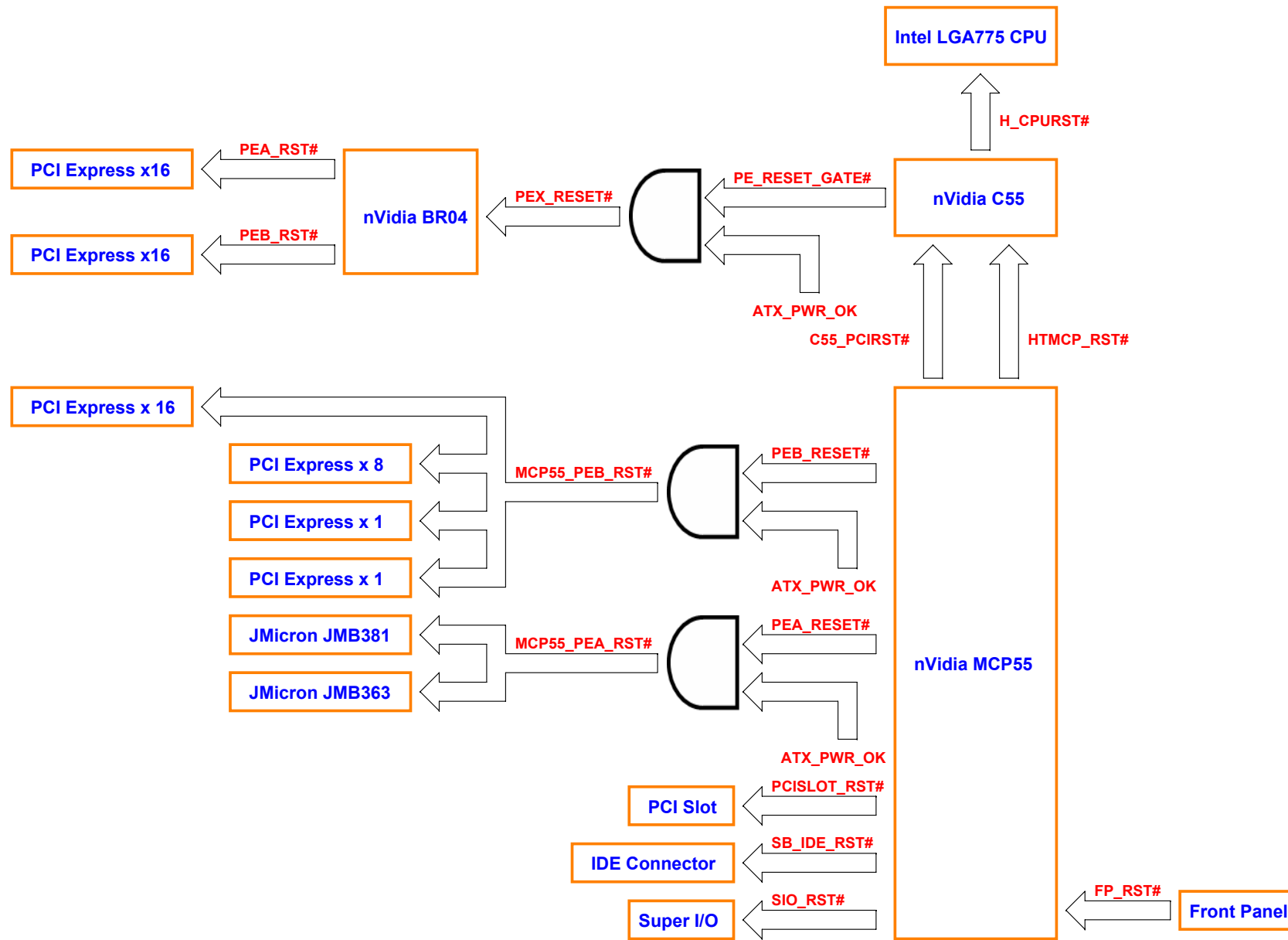
MCP55 GPIO Function

Pin Name	Function Description
GP10	USB Connector OC# Detect
GP6	LAN0_DISABLE#
GP7	LAN1_DISABLE#

Device Clock Signal

Signal	Device
CK_H_CPU# CK_H_CPU	C55 to CPU
HTMCP_DWNCLK0 HTMCP_DWNCLK0#	C55 to MCP55
HTMCP_UPCLK0 HTMCP_UPCLK0#	MCP55 to C55
PE_BR04_CLK PE_BR04_CLK#	C55 to BR04
BF_PE_CLK BF_PE_CLK#	C55 to Clock Buffer
PE_BR04_REFCLK PE_BR04_REFCLK#	Clock Buffer to BR04
PE_A_REFCLK PE_A_REFCLK#	Clock buffer to Express x 16 Primary Slot
PE_B_REFCLK PE_B_REFCLK#	Clock Buffer to Express x 16 Secondary Slot
MCPOUT_200MHZ MCPOUT_200MHZ#	MCP55 to C55
C55_25MHZ	MCP55 to C55
PE0SB_CLK PE0SB_CLK#	MCP55 to Express x 16 Slot
PE5SB_CLK PE5SB_CLK#	MCP55 to Express x 8 Slot
PE1SB_CLK PE1SB_CLK# PE2SB_CLK PE2SB_CLK#	MCP55 to PCI Express x 1 Slot
PE3SB_CLK PE3SB_CLK#	MCP55 to JMicron JMB363 eSATA Controller
PE4SB_CLK PE4SB_CLK#	MCP55 to JMicron JMB381 IEEE1394a Controller
PCI_CLK0	MCP55 to PCI Slot
SIO_PCLK	MCP55 to FinTek 71883FG Super I/O
LPC_PCLK	MCP55 to JTPM Pin Header
PE_100M_LAN0 PE_100M_LAN0#	MCP55 to LAN1
PE_100M_LAN1 PE_100M_LAN1#	CLOCK BUFFER to LAN2

System Reset Map



- 2007-12-17 Modify to Version 2.0 for acer Beetle**
- Update circuit**
1. Change LAN connector to meet acer requirement -- page 25
 2. Change Audio connector to meet acer requirement -- page 27
 3. Add Audio De-pop circuit to meet acer requirement -- page 20,36
 4. Remove FDD and TPM -- page 29
 5. Add four system fan to meet acer requirement -- page 30
 6. Change USB connector to header -- page 34
 7. Modify the front panel header to meet acer requirement -- page 35
 8. Add 2x5 GPIO pin header to meet acer requirement -- page 20
1. Change PCIE X8 to PCI slot -- page 17,18,23

- 2007-12-18**
- 1.change PCI slot2 to PCIE X8(PCI_E6) -- page 17,18,23,24
 - 2.remove three system fan to meet acer requirement -- page 30

- 2007-12-19**
- 1.remove JCD1 to meet acer requirement -- page 27
 - 2.remove IDE2 to meet acer requirement -- page 28
 - 3.change R271&R274 to 10Kohm from 1Kohm -- page 25
 - 4.change C684&C686 to 22p from 0.1u -- page 25
 - 5.remove R358 -- page 27
 - 6.remove R395&R401 and change R357&R359 to suffuse from reserve -- page 27
 - 7.remove D10 and change pin21(U13) pin name -- page 27
 - 8.add C660&C679&C811&C812 470p Cap. -- page 27
 - 9.remove C616&C617&C621&C622 -- page 27
 - 10.change JSP1 connect for acer requirement -- page 27
 - 11.add R821&R822 -- page 27

- 2007-12-20**
- 1.change L4 to 30L600mA from 10uH100mA -- page 7

- 2007-12-24**
- 1.change FB12,FB13,FB14,FB15 footprint to 0402 from 0603 -- page 29
 - 2.4.remove CP49 -- page 29

- 2007-12-26**
- 1.change EC18 to 10uX5R from 4.7uX5R -- page 27
 - 2.change C854,C855,C852,C853,C850,C851 to 4.7uX5R from 10uX5R -- page 27
 - 3.change R382 to 324ohm from 300ohm -- page 27
 - 4.remove D6&R376&R377 -- page 27
 - 5.add R364&R365 -- page 27
 - 6.move R362 location between EC96 and L14 -- page 27
 - 7.move R361 location between EC97 and L15 -- page 27
 - 8.move R371 location between EC98 and L16 -- page 27
 - 9.move R370 location between EC99 and L17 -- page 27
 - 10.move R380 location between C852 and R823 -- page 27
 - 11.move R379 location between C853 and R824 -- page 27
 - 12.move R383 location between EC100 and L18 -- page 27
 - 13.move R384 location between EC101 and L19 -- page 27
 - 14.move R398 location between C850 and R821 -- page 27
 - 15.move R397 location between C851 and R822 -- page 27

- 2007-12-28**
- 01.Add serial resistor R666 (10k ohm) for Q53. -- Page. 31
 - 02.Don't stuff R48 (0 ohm) for Yorkfield CPU. -- Page. 4
 - 03.Change part number of Q65 to D03-2005K09-D07. -- Page. 4
 - 04.Change R302 & R303 from 22 ohm to 0 ohm. -- Page. 25
 - 05.Change C529, C531, C530 & C532 from 27pF to 22pF. -- Page. 25
 - 06.Change R191 & R201 from 22 ohm to 0 ohm. -- Page. 19
 - 07.Don't stuff Q7 & Q8. -- Page. 29
 - 08.Don't stuff R477 (For 7510-1.0 BOM select).
 - 09.Change footprint of RN50 & RN51 from 0402 to 0603. -- Page.26
 - 10.Reserve C830 & C833 (0.1uF/0402) for VCC5 to GND. -- Page.28, 29
 - 11.Reserve C921 (0.1uF/0402) for VCC1_2 to GND. -- Page.32

- 2007-12-31**
- 01.Add Q85,R242,R825 and R826 for front panel LED controller circuit. - page. 20

- 2008-01-02**
- 1.change LAN chip to MARVELL/88E8056(B1) from Realtek RTL8211BL-GR -- Page. 25
 - 2.add R900~R913 for remove RGMII interface -- Page. 19

- 2008-01-03**
- 1.change HEATPIPE P/N

- 2008-01-04**
- change super I/O to ITE IT8718F and circuit from FinTek F71882FG -- Page. 29
- remove parallel port did not pull up - Page29
- R509 change to 10K ohm and non-stuff R514. - Page29
- Remove R734 and short it directly - Page29
- Remove C678,C677,C669 and C668. - Page29
- Remove R491 - Page29
- R452, R460 and R480 non-stuff - Page29
- Modify VIN pin define(pin 13 for LED_VCC,pin 19 for PWM_WDT#) - Page29
- add pin 79 for LED_VSB use - Page29
- DTRA should change to pull low - Page29
- Remove SKTOCC#. - Page3
- Remove R236 and connect it to LPC_SMI#. - Page20
- Remove R228 and RGMII_RST# - Page20
- Remove DUAL_CTRL and R692 - Page31
- Remove THRM#. - Page20
- remove R366 and R667 - Page25
- change U36 and U46 pin 47 connct to VCC3 - Page25
- change R367 and R440 to 0ohm(resever) - Page25

- 2008-01-04**
- remove R366 and R667 - Page25
- change U36 and U46 pin 47 connct to VCC3 - Page25
- change R367 and R440 to 0ohm(resever) - Page25

- 2008-01-04**
- remove U45B and U50 - Page30
- remove R501,R502,C688,C928,R526,R527,C689,R239 of sysfan1 controller - Page30
- ADD U19 R169,R191,R549,C545,R546,C547,C548,R314,R311 for sysfan1 controller - Page30
- remove R505,R503,C692,C931,R528,R529,C867,R240 of sysfan2 controller - Page30
- ADD U20 R198,R200,C555,C551,C552,C553,C554,R312,R315 for sysfan2 controller - Page30
- CHANGE Q73 Q74 to N-P3057_TO252 from P-P06P03LCG_SOT89 - Page30


- 2008-01-07**
- change the R497 from 1% to 5% resistor - Page30
- Change the C880 to EC Cap(EC109_100uF) - Page30
- remove U20,C551,C553,C552,and system fan2 use U19 controller - Page30

- 2008-01-08**
- Add C995&C998 for 3VDUAL - Page25
- LAN chip pin40 and pin44 connect to 3VDUAL direct - Page25
- remove C993&C951 - Page25
- remove EC15 - Page25
- change EC100&EC101 to 100u from 10u - Page27
- add R450,R453,R454,R456,R458 pull high resistor - Page29
- move C950,C601,C622 location,between FB18 and C617 - Page25
- move C616,C947,C621 location,between FB19 and C602 - Page25
- move C991,C661,C941 location,between FB20 and C686 - Page25
- move C684,C978,C940 location,between FB21 and C685 - Page25
- change R504,R508 to 1Kohm5% from 1Kohm1% resistor - Page35

- 2008-01-09**
- swap RN38,RN58 pin connect for layout space - Page29
- remove AVDDL0,AVDDL1,VDD0,VDD1 net name - Page25

- 2008-01-10**
- ADD CP56,CP57,CP58 for EMI request
- REMOVE C254,C830 for EMI request

- 2008-01-11**
- ADD Q88,Q89,Q90,R310,R827,R316,R313,R829,R828,R830 -- Page20
- CHANGE JGPIO PIN CONNECT PIN2_NON USE,PIN4_GPIO14,PIN7_WHITE_LED,PIN8_BLUE_LED -- Page20



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Title

History

Size

Document Number

Rev

MS-7510

2.0

Date:

Saturday, January 12, 2008

Sheet

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